INNOVATIVE TEACHING

Faculty Name : **Dr. C. G. HEMAMALINI, Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.**

Method – I : **SEMINAR ASSIGNMENTS :**

Faculty : Dr. C. G. Hemamalini, Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

15CV71 - Municipal and Industrial Waste Water Engineering
Seminar on Assignment
7th Sem – Batch 2015-19

Topic - Disposal standards of different industrial effluents

The students of final year were given the assignment topic of disposal standards of different industrial effluents covering the different industries namely dairy industry, cement industry, pharmaceutical industry, petrochemical industry, textile industry, tannery industry, sugar industry, distillery industry, paint industry etc. The presentation includes process flow chart of industry, treatment methods and disposal standards. They presented using power point projection and submitted the write up in the assignment book.

INNOVATIVE TEACHING

Faculty Name : **Mr. SHASHIKUMAR M. HIREMATH**
Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

Method : **ON-SITE TEACHING:**

Faculty : Mr. Shashikumar M. Hiremath., Assistant Professor,
Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

15CV71 : Municipal and Industrial Wastewater Engineering

7th Sem – Batch 2016-20

Topic – Sewage Treatment Plant Process and Treatment Units

Final year 7th sem students were taken to the Sewage Treatment Plant of capacity 200 KLD site functioning within the campus of J.N.N. College of Engineering, Shivamogga on 27-09-2019. Students were made practically familiarise with the physical, chemical and biological treatment units and their functioning. Also a phytoremedian system of capacity 5KLD installed beside the STP is also visited by the students to be demonstrated practically the low cost treatment method for sewage using plants like cattail, water hyacinth, etc.

Method – III : DEMONSTRATION THROUGH WORKING MODELS:

Faculty : Dr. C. G. Hemamalini, Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

17CV33 - FLUID MECHANICS
DEMO IN FM LAB
3th Sem – Batch 2017-21

Topic – Demo on pressure and discharge measuring devices

The students of second year were taken to FM lab to explain about the principles of working of pressure measuring devices namely piezometer, differential manometer and pressure gauge and discharge measuring devices namely Venturimeter and Orifice meter. Also, they were shown different types of notches and orifice.

INNOVATIVE TEACHING

Method : **LIVE DEMO TEACHING**

Offline Faculty : Mr. Shashikumar M. Hiremath, Assistant Professor, , Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

5th Semester 'B' Section, B.E. (Civil) Students (2022-23) were taken to In campus Sewage Treatment Plant JNNCE on November. 29th and December 1st . 2022. The visit was to demonstrate the live treatment processes and working of wastewater treatment units onsite. The contents delivered are for the course Municipal Wastewater Engineering (18CV55). This type of onsite teaching will help students to interact with real time understanding of the contents.

18CV55 – MUNICIPAL WASTEWATER ENGINEERING

ONSITE TEACHING

5th Sem – Batch 2020-24

Topic – Sewage Treatment Plant Units and their Function

Method – IV : FLIPGRID ASSIGNMENT :

Faculty : Dr. C. G. Hemamalini, Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

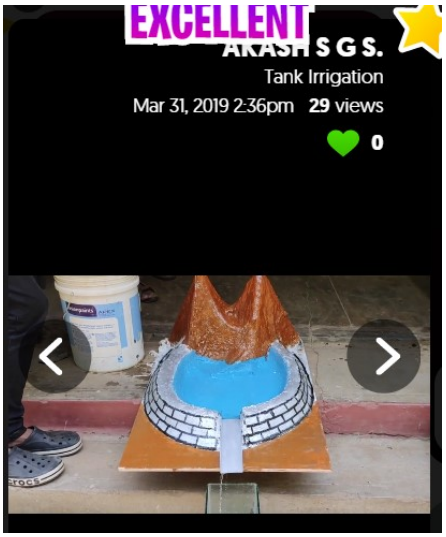
4th semester B Sec students (2018-19) have given the model making event on 26-02-2019 as assignment for the course Applied Hydraulics (17CV43). An online account in the flipgrid is created and added the students to post their model videos. Also they presented their models in the lab. Following link is for public access in our college website. https://flipgrid.com/caa1ca54

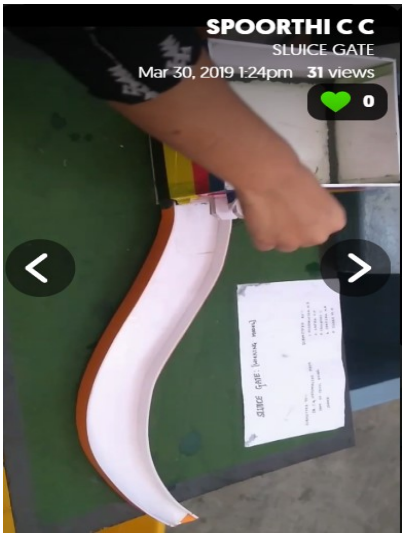
17CV43 - FLUID MECHANICS

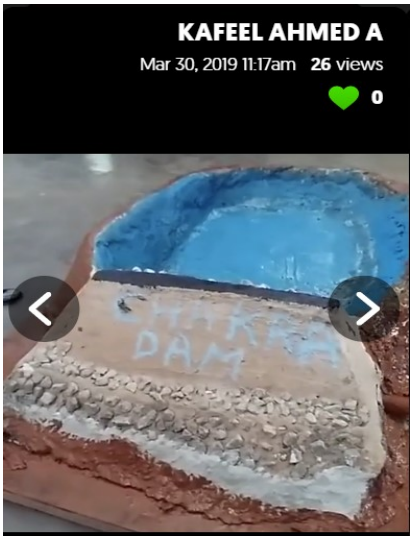
MODEL MAKING EVENT

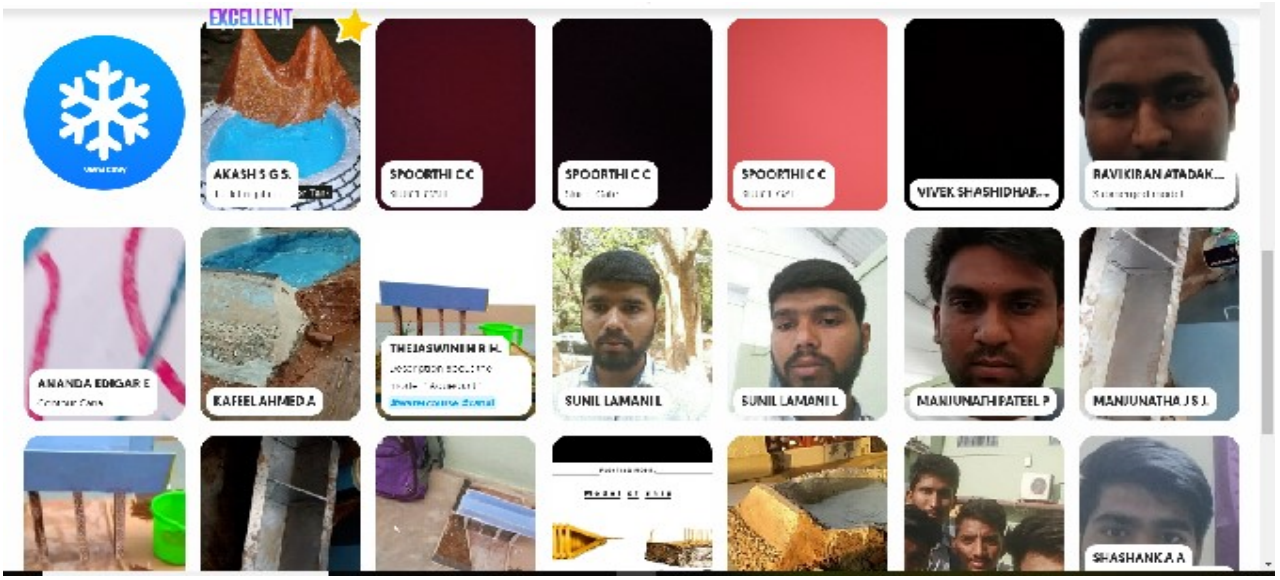
4th Sem – Batch 2017-21

Topic – Hydraulic Structures









INNOVATIVE TEACHING

Method : **ONSITE TEACHING**

Offline Faculty : Mr. Shashikumar M. Hiremath, Assistant Professor, , Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

5th Semester 'B' Section, B.E. (Civil) Students (2021-22) were taken to In campus Sewage Treatment Plant JNNCE on January, 11th 2022. The visit was to demonstrate the live treatment processes and working of wastewater treatment units onsite. The contents delivered are for the course Municipal Wastewater Engineering (18CV55). This type of onsite teaching will help students to interact with real time understanding of the contents.

18CV55 – MUNICIPAL WASTEWATER ENGINEERING

ONSITE TEACHING

5th Sem – Batch 2019-23

Topic – Wastewater Treatment Plant Units and their Function

INNOVATIVE TEACHING

Faculty Name : **Mr. BHUVAN KUMAR V. S.,**
Assistant Professor, Department of Civil Engineering,
J.N.N. College of Engineering, Shivamogga.

Method : **ON-SITE TEACHING:**

Faculty : Mr. Bhuvan Kumar V. S., Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

15CV61 : Construction Management and Entrepreneurship

6th Sem – Batch 2015-19

Topic – Construction Stages and Materials Management

Students are taken to the ongoing construction project sites/construction materials vendor shops for practical demonstration of various construction stages, material management, to gather information about the market values of the various constructional materials etc.

INNOVATIVE TEACHING

Faculty Name : **Mr. RABINANDAN J.,**
Assistant Professor, Department of Civil Engineering,
J.N.N. College of Engineering, Shivamogga.

Method : **ON-SITE TEACHING:**

Faculty : Mr. Rabinandan J., Assistant Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

17CV34 – Advanced Surveying

4th Sem – Batch 2017-21

Topic – Staking out points and Alignment using Total Station

Students are taken to the ongoing construction project sites for practical demonstration of alignment of columns, staking out the points on the ground, surveying, various construction stages, to gather information.

INNOVATIVE TEACHING

Faculty Name : **Dr. KARTHIKA B. S.,**
Assiociate Professor, Department of Civil Engineering,
J.N.N. College of Engineering, Shivamogga.

Method : **ON-SITE TEACHING:**

Faculty : Dr. Karthika B. S., Assisociate Professor, Department of Civil Engineering, J.N.N. College of Engineering, Shivamogga.

17CV34 – Basic Surveying

3rd Sem – Batch 2017-21

Topic – Building Centre Line Marking

Students are taken to the ongoing construction project sites for practical demonstration of Building centre line marking, surveying, various construction stages, to gather information.

Visvesvaraya Technological University

BELAGAVI, KARNATAKA

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ

ಬೆಳಗಾವಿ, ಕರ್ನಾಟಕ

OS CASE STUDY ON

"RTOS"

Submitted by

4JN18IS053	PANNAGASHREE
4JN18IS088	SHEETHAL R
4JN19IS001	AADHI MAHISHI J
4JN19IS002	ABDUL HAMEED
4JN19IS003	ADITHYA K R
4JN19IS004	ADITHYA NARAYAN
4JN19IS005	AMITHA S KRISHNA
4JN19IS006	ANIDUDH V SHASTRY
4JN19IS007	ANUSHA H Y
4JN19IS008	ARJUN V
4JN19IS009	ARPITHA V
4JN19IS010	ARPITHA A T
4JN19IS011	ARUNDHATHI G V

Under the guidance of

JYOTHI K

Dept. of IS&E,

JNNCE, Shivamogga

Department of Information Science & Engineering

J N N College of Engineering

Shivamogga - 577 204

2020-21

1. INTRODUCTION

A real-time operating system (RTOS) is an operating system (OS) intended to serve real time application requests. It must be able to process data as it comes in, typically without buffering delays. Processing time requirements are measured in tenths of seconds or shorter. Real-time operating systems have evolved over the years from being simple executives using cyclic scheduling to the current feature-rich operating environments. The standardization of POSIX 1003.1, ISO/IEC 9945-1 (real-time extensions to POSIX) has contributed significantly to this evolution, however, the specification leaves plenty of room for individual implementations to both interpret and specialize their RTOSs. Accordingly, there has been a proliferation of both commercial and free RTOSs, notably, the ITRON OS, the OSEK-VDX OS specification, commercial RTOSs like VxWorks, VRTX, LynxOS, OSE and QNX, and free RTOSs like RT-Linux (RTAI), and Windows CE. The goal of the work reported in this paper is to draw the real-time systems practitioner and researcher's attention to these choices and bring out the similarities and differences among them.

2. DEFINITION

Real-time operating system (RTOS) is an operating system intended to serve real time application that process data as it comes in, mostly without buffer delay. The full form of RTOS is Real time operating system.

In a RTOS, Processing time requirement are calculated in tenths of seconds increments of time. It is time-bound system that can be defined as fixed time constraints. In this type of system, processing must be done inside the specified constraints. Otherwise, the system will fail.

3. REASONS for using RTOS

Here are important reasons for using RTOS:

- It offers priority-based scheduling, which allows you to separate analytical processing from non-critical processing.
- The Real time OS provides API functions that allow cleaner and smaller application code.
- Abstracting timing dependencies and the task-based design results in fewer interdependencies between modules.
- RTOS offers modular task-based development, which allows modular task-based testing.
- The task-based API encourages modular development as a task, will typically have a clearly defined role. It allows designers/teams to work independently on their parts of the project.
- An RTOS is event-driven with no time wastage on processing time for the event which is not occur.

4. CHARACTERISTICS

A key characteristic of an RTOS is the level of its consistency concerning the amount of time it takes to accept and complete an application's task; the variability is 'jitter'.

A 'hard' real-time operating system (Hard RTOS) has less jitter than a 'soft' real-time operating system (Soft RTOS). The late answer is a wrong answer in a hard RTOS while a late answer is acceptable in a soft RTOS. The chief design goal is not high throughput, but rather a guarantee of a soft or hard performance category. An RTOS that can usually or generally meet a deadline is a soft real-time OS, but if it can meet a deadline deterministically it is a hard real-time OS.

An RTOS has an advanced algorithm for scheduling. Scheduler flexibility enables a wider, computer-system orchestration of process priorities, but a real-time OS is more frequently dedicated to a narrow set of applications. Key factors in a real-time OS are minimal interrupt latency and minimal thread switching latency; a real-time OS is valued more for how quickly or how predictably it can respond than for the amount of work it can perform in a given period of time.

5. Design philosophies

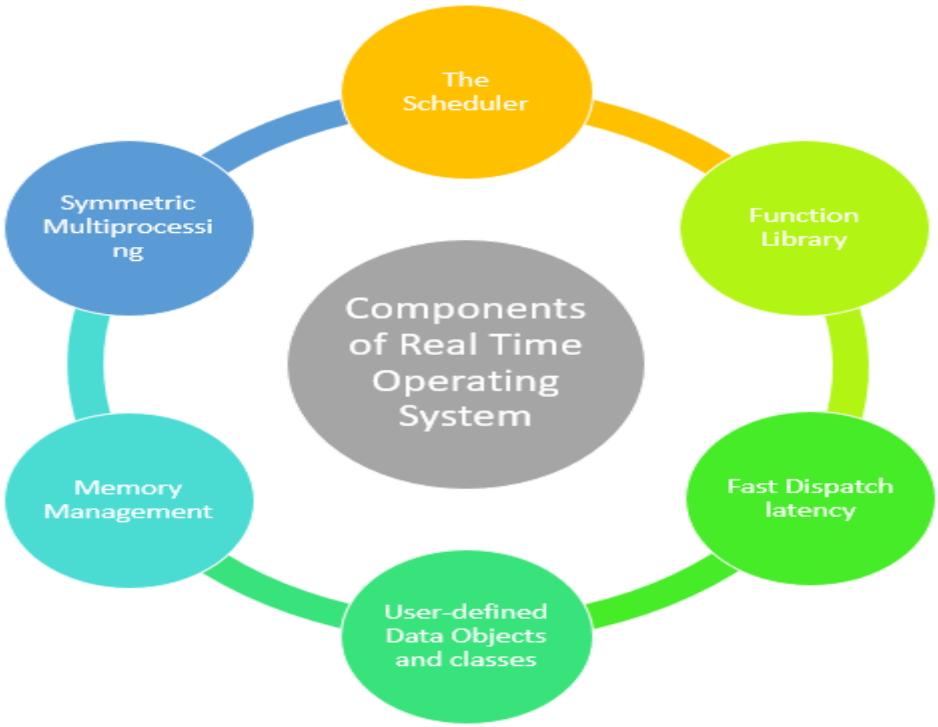
An RTOS is an operating system in which the time taken to process an input stimulus is less than the time lapsed until the next input stimulus of the same type.

The most common designs are:

- **Event-driven –** switches tasks only when an event of higher priority needs servicing; called preemptive priority, or priority scheduling.
- **Time-sharing** – switches tasks on a regular clocked interrupt, and on events; called round robin.

Time sharing designs switch tasks more often than strictly needed, but give smoother multitasking, giving the illusion that a process or user has sole use of a machine.
Early CPU designs needed many cycles to switch tasks during which the CPU could do nothing else useful. Because switching took so long, early OSes tried to minimize wasting CPU time by avoiding unnecessary task switching.

6. Components of RTOS



Here, are important Component of RTOS

The Scheduler: This component of RTOS tells that in which order, the tasks can be executed which is generally based on the priority.

Symmetric Multiprocessing (SMP): It is a number of multiple different tasks that can be handled by the RTOS so that parallel processing can be done.

Function Library: It is an important element of RTOS that acts as an interface that helps you to connect kernel and application code. This application allows you to send the requests to the Kernel using a function library so that the application can give the desired results.

Memory Management: this element is needed in the system to allocate memory to every program, which is the most important element of the RTOS.

Fast dispatch latency: It is an interval between the termination of the task that can be identified by the OS and the actual time taken by the thread, which is in the ready queue, that has started processing.

User-defined data objects and classes: RTOS system makes use of programming languages like C or C++, which should be organized according to their operation.

7. Classification of Events in Real-time System

Events in a real-time System are the actions or the result of the actions that are generated by the system or the environment. An event in a real-tie system is either a instantaneous or may have certain duration. The classification of events in a real-time system is based on different theories. Once the events in real-time system are classified thereafter timing constraints are categorized accordingly.

Classification of Events :

1. On the basis of generation :
An event in a real-time system may be generated by either system of the environment. On this basis events are classified into two categories:

- **Stimulus Events –**
  In a real-time system, stimulus events are generated by the environment. Stimulus events act on the computer system. Stimulus events are aperiodic and asynchronous. These events are not generated for a response. Stimulus events may be instantaneous or may have some duration.

  Example :

  1. Typing on keyboard is a stimulus event that acts on the computer system.
  2. Measuring of temperature in a plant.

- **Response Events –**
  In a real-time system, response events are generated by the computer system. These events act on the environment. These events are generated in response of stimulus events. Response events may be periodic or aperiodic. These events are generated for a response. Response events are generally instantaneous events.
  Example :
  1. Alarm ringing at 4 o'clock is a response event.
  2. Switching off the induction at temperature exceeding 100 degree.

2. On the basis of duration :
An event in a real-time system may be instantaneous or may have some duration. On this basis events in a real-time system are classified into two categories:

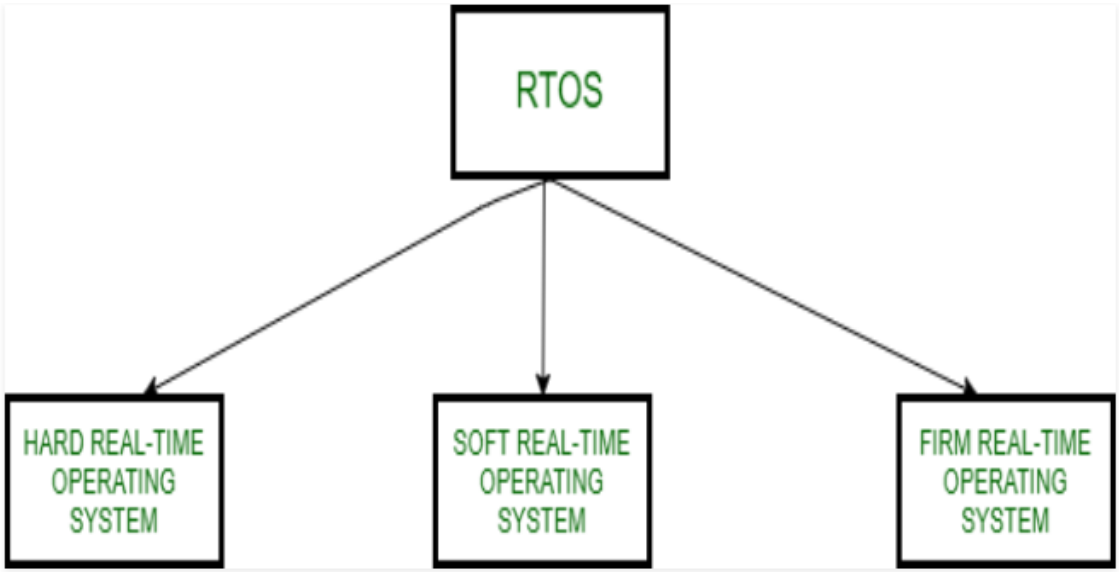
- **Instantaneous Events –**
  In a real-time system, instantaneous events are the events having duration time zero. These events may be generated by the environment or the computer system but these are generated at instant time. Instantaneous events may be stimulus events or response events.
  Example :
  1. Pressing a key at a instant.
  2. Display of alert notice at any instant.

- **Durational Events –**
  In a real-time system, duration events are the events having duration time greater than zero. These events may be generated by the environment or the computer system but these events have some duration time. Duration events may be stimulus events or response events.

Example :

1. Measuring of temperature is a durational event.
2. All the computational events inside computer system are durational events.

8. Types of RTOS



Three types of RTOS systems are:

Hard Real Time :

In Hard RTOS, the deadline is handled very strictly which means that given task must start executing on specified scheduled time, and must be completed within the assigned time duration.

Example: Medical critical care system, Aircraft systems, etc.

Firm Real time:

These type of RTOS also need to follow the deadlines. However, missing a deadline may not have big impact but could cause undesired affects, like a huge reduction in quality of a product.

Example: Various types of Multimedia applications.

Soft Real Time:

Soft Real time RTOS, accepts some delays by the Operating system. In this type of RTOS, there is a deadline assigned for a specific job, but a delay for a small amount of time is acceptable. So, deadlines are handled softly by this type of RTOS.

Example: Online Transaction system and Livestock price quotation System.

9. Terms used in RTOS

Here, are essential terms used in RTOS:

- **Task –** A set of related tasks that are jointly able to provide some system functionality.
- **Job –** A job is a small piece of work that can be assigned to a processor, and that may or may not require resources.
- **Release time of a job –** It's a time of a job at which job becomes ready for execution.
- **Execution time of a job:** It is time taken by job to finish its execution.
- **Deadline of a job:** It's time by which a job should finish its execution.
- **Processors:** They are also known as active resources. They are important for the execution of a job.
- **Maximum It is the** allowable response time of a job is called its relative deadline.
- **Response time of a job:** It is a length of time from the release time of a job when the instant finishes.
- **Absolute deadline:** This is the relative deadline, which also includes its release time.

10. Features of RTOS

Here are important features of RTOS:

- Occupy very less memory
- Consume fewer resources
- Response times are highly predictable

- Unpredictable environment
- The Kernel saves the state of the interrupted task ad then determines which task it should run next.
- The Kernel restores the state of the task and passes control of the CPU for that task.

11. Factors of RTOS

Performance: it is the most important factor needed to be considered while choosing for a RTOS. As we know RTOS is a system which gives us guarantee about the data within a given frame of time. So it does not take care of our PC whatever is happening with it. So we must have to keep a check on its performance.
• **Unique features**: A good RTS must be scalable and it has some extra features like efficient protection of the memory of the system, how it operates to execute commands etc.. So, we have to evaluate these features so that our system can run effectively and efficiently.
• **Your IT team**: A good RTOS is that which works in the favor of our IT team. Here, favor means reducing the labor intensity of the team. If this intensity of the team get reduced, then the team can concentrate on other factors. So we have to decide those RTOS, through which our team can easily familiar with.
• **Middleware**: if there will be no middleware support in RTOS, then the problem of time-consuming integration of processes will take place. Here, middleware support means those components which can be integrated with our RTOS.
Advantages of real time operating system
• **Error free**: Real time operating systems are error-free. So there is no chance of getting an error when we are performing the task.
• **Maximum Consumption**: we can achieve maximum consumption by using RTOS. It keeps all the devices active and produces more output by making use of all the resources.
• **Embedded system usage**: As the programs of the RTOS are of small size. So, we make use of RTOS in embedded systems.
• **Task shifting**: In RTOS, shifting time of the tasks is very small.
• **24/7 performance**: RTOS is best used for those applications which run constantly or you can say that which runs for 24 hours and 7 days in a week. This is possible because of fewer shifting of tasks so that it can give maximum output.

• **Application focus**: in RTOS, a very few tasks are managed so that exact results can be given by the system. It gives very less importance to those applications which are in waiting state.

12. Scheduling

In typical designs, a task has three states:

i. Running (executing on the CPU);

ii. Ready (ready to be executed);

iii. Blocked (waiting for an event, I/O for example).

Most tasks are blocked or ready most of the time because generally only one task can run at a time per CPU. The number of items in the ready queue can vary greatly, depending on the number of tasks the system needs to perform and the type of scheduler that the system uses. On simpler non-preemptive but still multitasking systems, a task has to give up its time on the CPU to other tasks, which can cause the ready queue to have a greater number of overall tasks in the ready to be executed state (resource starvation).

Usually, the data structure of the ready list in the scheduler is designed to minimize the worst-case length of time spent in the scheduler's critical section, during which preemption is inhibited, and, in some cases, all interrupts are disabled, but the choice of data structure depends also on the maximum number of tasks that can be on the ready list.

If there are never more than a few tasks on the ready list, then a doubly linked list of ready tasks is likely optimal. If the ready list usually contains only a few tasks but occasionally contains more, then the list should be sorted by priority. That way, finding the highest priority task to run does not require iterating through the entire list. Inserting a task then requires walking the ready list until reaching either the end of the list, or a task of lower priority than that of the task being inserted.

Care must be taken not to inhibit preemption during this search. Longer critical sections should be divided into small pieces. If an interrupt occurs that makes a high priority task ready during the insertion of a low priority task, that high priority task can be inserted and run immediately before the low priority task is inserted.

The critical response time, sometimes called the flyback time, is the time it takes to queue a new ready task and restore the state of the highest priority task to running. In a well-designed RTOS, readying a new task will take 3 to 20 instructions per ready-queue entry, and restoration of the highest-priority ready task will take 5 to 30 instructions.

In more advanced systems, real-time tasks share computing resources with many non-real-time tasks, and the ready list can be arbitrarily long. In such systems, a scheduler ready list implemented as a linked list would be inadequate.

Algorithms

Some commonly used RTOS scheduling algorithms are:

- Cooperative scheduling
- Preemptive scheduling
  - Rate-monotonic scheduling
  - Round-robin scheduling
  - Fixed priority pre-emptive scheduling, an implementation of preemptive time slicing
  - Fixed-Priority Scheduling with Deferred Preemption
  - Fixed-Priority Non-preemptive Scheduling
  - Critical section preemptive scheduling
  - Static time scheduling
- Earliest Deadline First approach
- Stochastic digraphs with multi-threaded graph traversal

13. Memory allocation

Memory allocation is more critical in a real-time operating system than in other operating systems.
First, for stability there cannot be memory leaks (memory that is allocated but not freed after use). The device should work indefinitely, without ever needing a reboot. For this reason, dynamic memory allocation is frowned upon.[*citation needed*] Whenever possible, all required memory allocation is specified statically at compile time. Another reason to avoid dynamic memory allocation is memory fragmentation. With frequent allocation and releasing of small chunks of memory, a situation may occur where available memory is divided into several sections and the RTOS is incapable of allocating a large enough continuous block of memory, although there is enough free memory. Secondly, speed of allocation is important. A standard memory

allocation scheme scans a linked list of indeterminate length to find a suitable free memory block,[5] which is unacceptable in an RTOS since memory allocation has to occur within a certain amount of time.

Because mechanical disks have much longer and more unpredictable response times, swapping to disk files is not used for the same reasons as RAM allocation discussed above.

The simple fixed-size-blocks algorithm works quite well for simple embedded systems because of its low overhead.

14. Intertask communication and resource Sharing

A multitasking operating system like Unix is poor at real-time tasks. The scheduler gives the highest priority to jobs with the lowest demand on the computer, so there is no way to ensure that a time-critical job will have access to enough resources. Multitasking systems must manage sharing data and hardware resources among multiple tasks. It is usually unsafe for two tasks to access the same specific data or hardware resource simultaneously.

There are three common approaches to resolve this problem:

i. Temporarily masking/disabling interrupts:

General-purpose operating systems usually do not allow user programs to mask (disable) interrupts, because the user program could control the CPU for as long as it wishes. Some modern CPUs do not allow user mode code to disable interrupts as such control is considered a key operating system resource. Many embedded systems and RTOSs, however, allow the application itself to run in kernel mode for greater system call efficiency and also to permit the application to have greater control of the operating environment without requiring OS intervention.

On single-processor systems, an application running in kernel mode and masking interrupts is the lowest overhead method to prevent simultaneous access to a shared resource. While interrupts are masked and the current task does not make a blocking OS call, the current task has *exclusive* use of

the CPU since no other task or interrupt can take control, so the critical section is protected. When the task exits its critical section, it must unmask interrupts; pending interrupts, if any, will then execute. Temporarily masking interrupts should only be done when the longest path through the critical section is shorter than the desired maximum interrupt latency. Typically this method of protection is used only when the critical section is just a few instructions and contains no loops. This method is ideal for protecting hardware bit-mapped registers when the bits are controlled by different tasks.

ii. Mutexes

When the shared resource must be reserved without blocking all other tasks (such as waiting for Flash memory to be written), it is better to use mechanisms also available on general-purpose operating systems, such as a mutex and OS-supervised interprocess messaging. Such mechanisms involve system calls, and usually invoke the OS's dispatcher code on exit, so they typically take hundreds of CPU instructions to execute, while masking interrupts may take as few as one instruction on some processors. A (non-recursive) mutex is either **locked** or unlocked. When a task has locked the mutex, all other tasks must wait for the mutex to be unlocked by its *owner* - the original thread. A task may set a timeout on its wait for a mutex. There are several well-known problems with mutex based designs such as priority inversion and deadlocks.

In priority inversion a high priority task waits because a low priority task has a mutex, but the lower priority task is not given CPU time to finish its work. A typical solution is to have the task that owns a mutex 'inherit' the priority of the highest waiting task. But this simple approach gets more complex when there are multiple levels of waiting: task *A* waits for a mutex locked by task *B*, which waits for a mutex locked by task *C*. Handling multiple levels of inheritance causes other code to run in high priority context and thus can cause starvation of medium-priority threads. In a deadlock, two or more tasks lock mutex without timeouts and then wait forever for the other task's mutex, creating a cyclic dependency. The simplest deadlock scenario occurs when two tasks alternately lock two mutex, but in the opposite order. Deadlock is prevented by careful design.

iii. Message passing

The other approach to resource sharing is for tasks to send messages in an organized message passing scheme. In this paradigm, the resource is managed directly by only one task. When another task wants to interrogate or manipulate the resource, it sends a message to the managing task.

Although their real-time behavior is less crisp than semaphore systems, simple message-based systems avoid most protocol deadlock hazards, and are generally better-behaved than semaphore systems. However, problems like those of semaphores are possible. Priority inversion can occur when a task is working on a low-priority message and ignores a higher-priority message (or a message originating indirectly from a high priority task) in its incoming message queue. Protocol deadlocks can occur when two or more tasks wait for each other to send response messages.

15. Interrupt handler and the scheduler

Since an interrupt handler blocks the highest priority task from running, and since real-time operating systems are designed to keep thread latency to a minimum, interrupt handlers are typically kept as short as possible. The interrupt handler defers all interaction with the hardware if possible; typically all that is necessary is to acknowledge or disable the interrupt (so that it won't occur again when the interrupt handler returns) and notify a task that work needs to be done. This can be done by unblocking a driver task through releasing a semaphore, setting a flag or sending a message. A scheduler often provides the ability to unblock a task from interrupt handler context.

An OS maintains catalogues of objects it manages such as threads, mutexes, memory, and so on. Updates to this catalogue must be strictly controlled. For this reason, it can be problematic when an interrupt handler calls an OS function while the application is in the act of also doing so. The OS function called from an interrupt handler could find the object database to be in an inconsistent state because of the application's update. There are two major approaches to deal with this problem: the unified architecture and the segmented architecture. RTOSs implementing the unified architecture solve the problem by simply disabling interrupts while the internal catalogue is updated. The downside of this is that interrupt latency increases, potentially losing interrupts. The segmented architecture does not make direct OS calls but delegates the OS related work to a separate handler. This handler runs at a higher priority than any thread but lower than the interrupt handlers. The advantage of this architecture is that it adds very few cycles to interrupt latency. As a result, OSes which implement the segmented architecture are more predictable and can deal with higher interrupt rates compared to the unified architecture.[*citation needed*]

Similarly, the System Management Mode on x86 compatible Hardware can take a lot of time before it returns control to the operating system.

16. Timing Constraints in RTOS

Timing constraints is a vital attribute in real-time systems. Timing constraints decides the total correctness of the result sin real-time systems. The correctness of results in real-time system does not depends only on logical correctness but also the result should be obtained within the time constraint.
There might be several events happening in real time system and these events are scheduled by schedulers using timing constraints.

Classification of Timing Constraints :

Timing constraints associated with the real-time system is classified to identify the different types of timing constraints in a real-time system. Timing constraints are broadly classified into two categories:

1.Performance Constraints :
The constraints enforced on the response of the system is known as Performance Constraints. This basically describes the overall performance of the system. This shows how quickly and accurately the system is responding. It ensures that the real-time system performs satisfactorily.

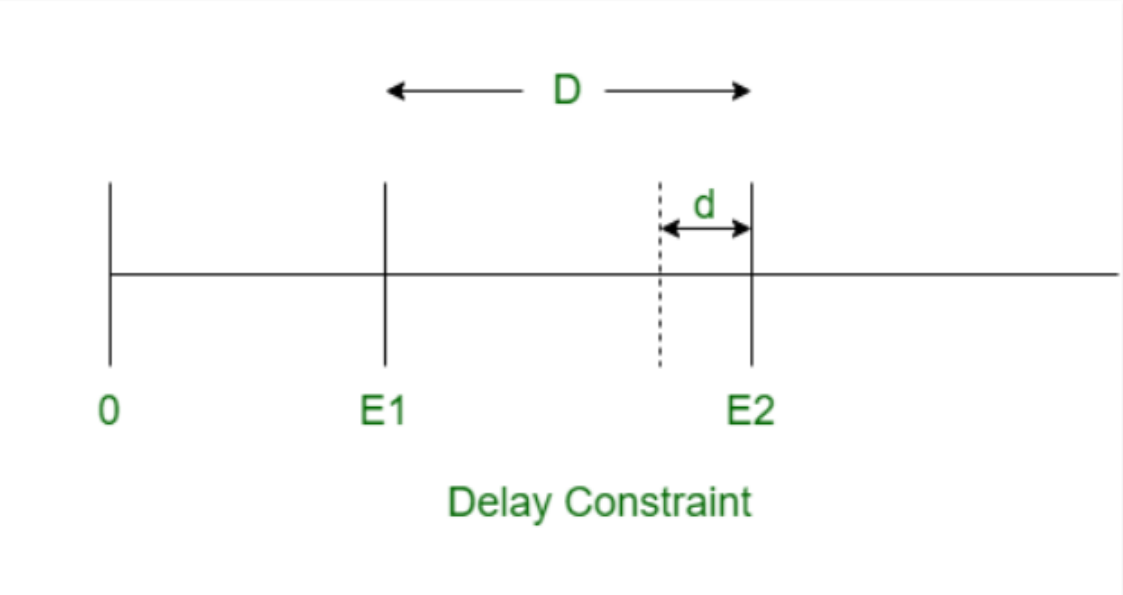
2. Behavioral Constraint :

The constraints enforced on the stimuli generated by the environment is known as Behavioral Constraints. This basically describes the behavior of the environment. It ensures that the environment of a system is well behaved.

Further, the both performance and behavioral constraints are classified into three categories: Delay Constraint, Deadline Constraint, and Duration Constraint. These are explained as following below.

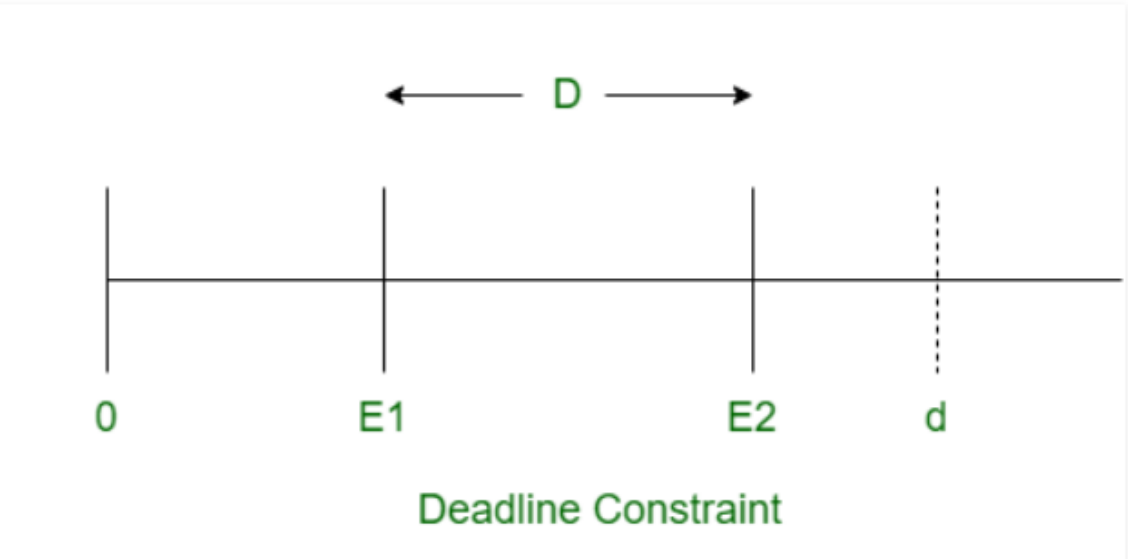
1.Delay Constraint –
A delay constraint describes the minimum time interval between occurrence of two consecutive events in the real-time system. If an event occurs before the delay constraint, then it is called a delay violation. The time interval between occurrence of two events should be greater than or equal to delay constraint.
If D is the actual time interval between occurrence of two events and d is the delay constraint, then

D >= d



2.Deadline Constraint –
A deadline constraint describes the maximum time interval between occurrence of two consecutive events in the real-time system. If an event occurs after the deadline constraint, then the result of event is considered incorrect. The time interval between occurrence of two events should be less than or equal to deadline constraint.
If D is the actual time interval between occurrence of two events and d is the deadline constraint, then

D <= d



3.Duration Constraint –
Duration constraint describes the duration of an event in real-time system. It describes the minimum and maximum time period of an event. On this basis it is further classified into two types:

- **Minimum Duration Constraint:** It describes that after the initiation of an event, it can not stop before a certain time.
- **Maximum Duration Constraint:** It describes that after the starting of an event, it must end before a certain time.

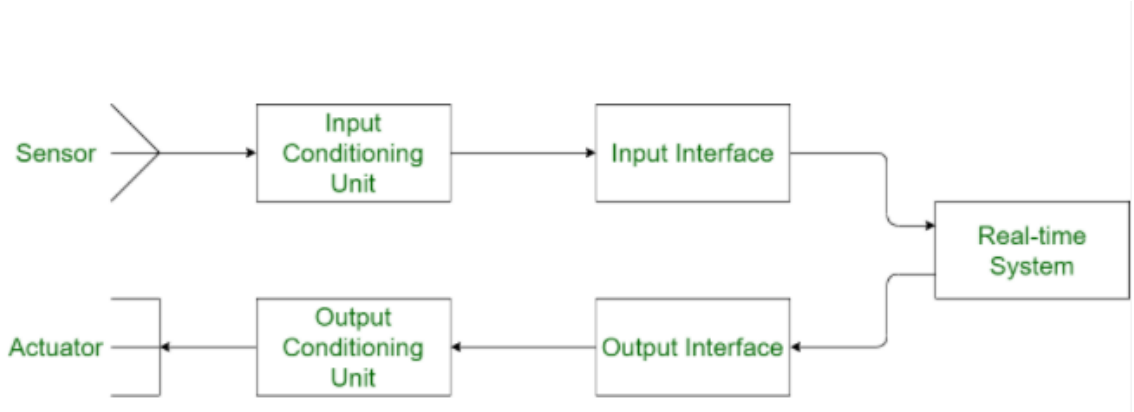
17. Basic Model of a RTOS

Real-time System is a system that is used for performing some specific tasks. These tasks are related with time constraints and need to be completed in that time interval.

Basic Model of a Real-time System:

The basic model of a real-time system presents the overview of all the components involved in a real-time system. Real-time system includes various hardware and software embedded in a such a way that the specific tasks can be performed in the time constraints allowed. The accuracy and correctness involved in real-time system makes the model complex. There are various models of real-time system which are more complex and are hard to understand. Here we will discuss a basic model of real-time system which has some commonly used terms and hardware.

Following diagram represents a basic model of Real-time System:



Sensor:
Sensor is used for the conversion of some physical events or characteristics into the electrical signals. These are hardware devices that that takes the input from environment and gives to the system by converting it. For example, a thermometer takes the temperature as physical characteristic and then converts it into electrical signals for the system.

Actuator:
Actuator is the reverse device of sensor. Where sensor converts the physical events into electrical signals, actuator does the reverse. It converts the electrical signals into the physical events or characteristics. It takes the input from the output interface of the system. The output from the actuator may be in any from of physical action. Some of the commonly used actuator are motors and heaters.

Signal Conditioning Unit:
When the sensor converts the physical actions into electrical signals, then computer can't used them directly. Hence, after the conversion of physical actions into electrical signals, they is need of conditioning. Similarly while giving the output when electrical signals are sent to the actuator, then also conditioning is required.
Therefore, Signal conditioning is of two types:

- **Input Conditioning Unit:** It is used for conditioning the electrical signals coming from sensor.
- **Output Conditioning Unit:** It is used for conditioning the electrical signals coming from the system.

Interface Unit:
Interface units are basically used for the conversion of digital to analog and vice-versa. Signals coming from the input conditioning unit are analog and the system does the operations on digital signals only, then the interface unit is used to change the analog signals to digital signals. Similarly, while

transmitting the signals to output conditioning unit the interface of signals are changed i.e. from digital to analog.
On this basis, Interface unit is also of two types:

- **Input Interface:** It is used for conversion of analog signals to digital.
- **Output Interface:** It is used for conversion of digital signals to analog.

18.Difference between in GPOS and RTOS

General - Purpose Operating System (GPOS)	Real-Time Operating System (RTOS)
It used for desktop pc, laptop.	It applied for the embedded application.
Process-based Scheduling used.	Time-based scheduling used like round robin.
Interrupt latency is not considered as much crucial as in RTOS.	Interrupt lag is minimal, measured in few microseconds.
No priority inversion mechanism is present in the system.	Priority inversion mechanism is current.Once priority set by the programmer, it can't be changed by the system itself.
Kernel operations may or may not be preempted.	Kernel operation can be preempted.

19.Applications of Real Time Operating System

Real-time systems are used in:

- Airlines reservation system.
- Air traffic control system.
- Systems that provide immediate updating.
- Used in any system that provides up to date and minute information on stock prices.
- Defense application systems like RADAR.
- Networked Multimedia Systems
- Command Control Systems
- Internet Telephony
- Anti-lock Brake Systems
- Heart Pacemaker

20.Disadvantages of RTOS

Here, are drawbacks/cons of using RTOS system:

- RTOS system can run minimal tasks together, and it concentrates only on those applications which contain an error so that it can avoid them.
- RTOS is the system that concentrates on a few tasks. Therefore, it is really hard for these systems to do multi-tasking.
- Specific drivers are required for the RTOS so that it can offer fast response time to interrupt signals, which helps to maintain its speed.
- Plenty of resources are used by RTOS, which makes this system expensive.
- The tasks which have a low priority need to wait for a long time as the RTOS maintains the accuracy of the program, which are under execution.
- Minimum switching of tasks is done in Real time operating systems.
- It uses complex algorithms which is difficult to understand.
- RTOS uses lot of resources, which sometimes not suitable for the system.

21.CHALLENGES

RTOS developers face following challenges :

Importance of time to market, Comparing design outcomes, Avoiding overqualified RTOS, Problem of delays in embedded applications.

These are some of the prominent RTOS that currently exist in the Market

Name	License	Platforms
FreeRTOS	Modified GNU GPL	ARM, AVR, AVR32, ColdFire, HCS12, IA-32, Cortex-M3, MicroBlaze, MSP430, PIC, PIC32, Renesas H8/S, 8052, STM32, EFM32
LynxOS	Proprietary	Motorola 68010, x86/IA-32, ARM, Freescale PowerPC, PowerPC 970, LEON
RTLinux	GNU GPL	Same as Linux
TI-RTOS	BSD license	Primarily Texas Instruments: MSP430, MSP432, C2000, C5000, C6000, TI's ARM families (Cortex M3/4F, Cortex R4, Cortex A8, Cortex A15), SimpleLink Wireless MCUs (CC2xxx, CC3xxx)
ThreadX	Proprietary	ARC, ARM/Thumb, AVR32, BlackFin, 680x0-ColdFire, H8- 300H, Luminary Micro Stellaris, M-CORE, MicroBlaze, PIC24-dsPIC, PIC32, MIPS, V8xx, Nios II, PowerPC, SH, SHARC, StarCore, STM32, StrongARM,

		TMS320C54x, TMS320C6x, x86/x386, XScale, Xtensa/Diamond, ZSP
VRTX	Proprietary	ARM, MIPS, PowerPC, RISC
VxWorks	Proprietary	ARM, IA-32, Intel 64, MIPS, PowerPC,SH-4, StrongARM, xScale
WindowsCE	Proprietary	x86, MIPS, ARM, SuperH

22.CONCLUSION

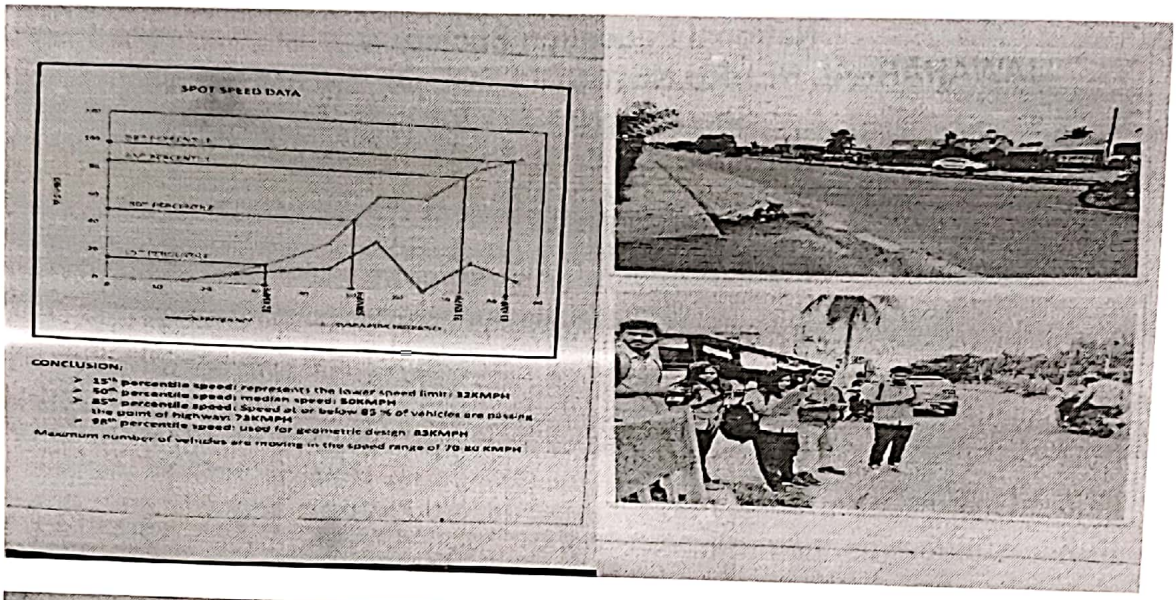
RTOS has evolved to a great extent in the recent years. Every RTOS has a distinct feature of its own. But the growth in this field is not fully utilized by the developers yet as most of the RTOS is licensed and highly expensive. Peripheral support and stack availability also varies widely from one RTOS to another. Out of the few available free/open source RTOS, support for proprietary protocols is minimal. Developers do not have the luxury of time to adapt RTOS to project requirements. Hence they are unwilling to change from their current working condition. It would be greatly beneficial if all the project requirements are listed in the beginning itself, so that the developer can ensure that the RTOS chosen has support for all the necessary drivers and protocols The domain of real-time operating system has a very active area of research in recent years. The field has seen many RTOS's being built with many different ideas, principles and paradigms. However, additional practical experience with such RTOS's is desirable.

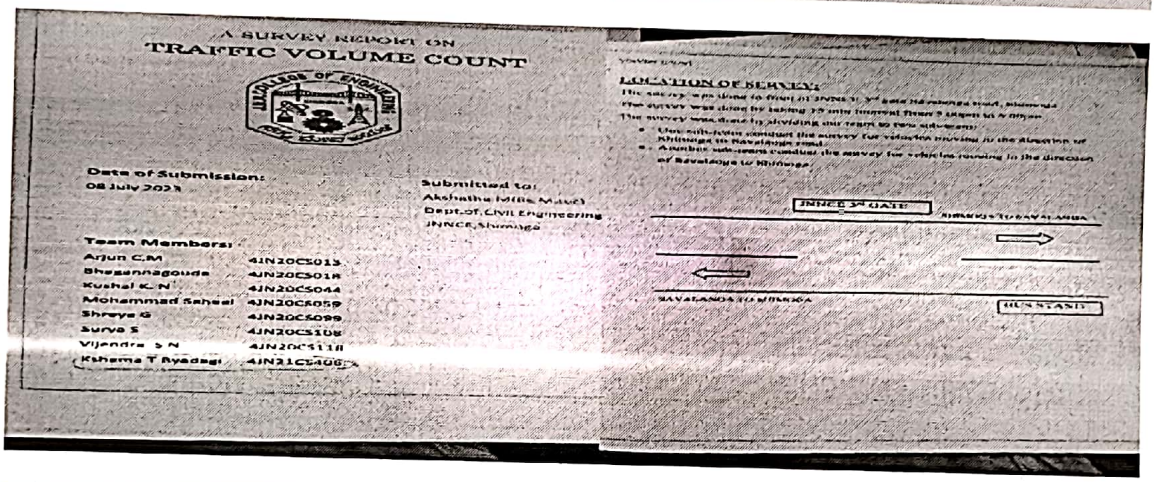
National Education Society ®
JAWAHARLAL NEHRU NEW COLLEGE OF ENGINEERING
Shivamogga - 577204
DEPARTMENT OF CIVIL ENGINEERING
PEDAGOGICAL INITIATIVE REPORT
18CV652 - Traffic Engineering
Field studies on Assignment
6th Sem – A section

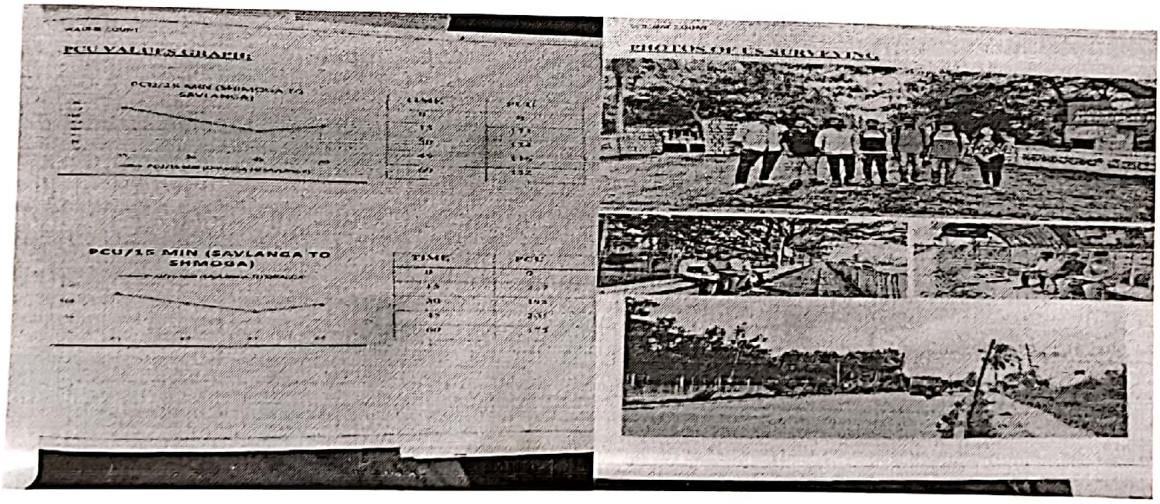
Topic – Various Traffic Studies on a given stretch in Shivamogga City

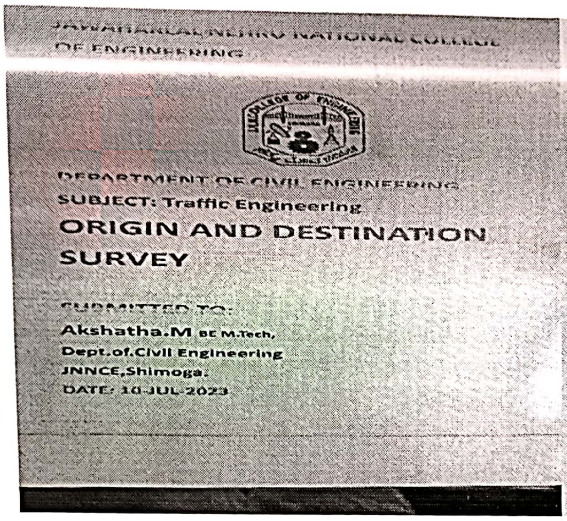
The students of 6th sem were made into different groups and were assigned few traffic studies as listed below. They were also given different road stretches and study area for carrying out traffic studies. They collected data from the field and analysed it separately and submitted the report as per the format. The sample copy is been attached below

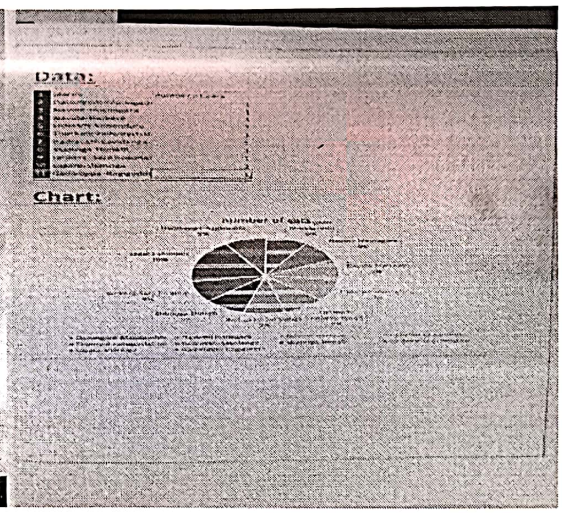
SL NO	ASSIGNMENT	CO
1	CARRYOUT VOLUME STUDIES AND GIVE MEASURES TO MAINTAINORDERLY MOVEMENT OF VEHICLES ON ROAD	2
2	CARRYOUT OD SURVEY AND GIVE THE MEASURE TO INCREASE THE TRAFFIC FLOW IN UNUSED ROADS	2
3	CARRY OUT SPOT SPEED STUDEIS AND GIVE THE AVERAGE SPEED WITH WHICH VEHICLES ARE MOVING ON THE SELECTED STRETECH	2
5	CARRYOUT PARKING STUDIES IN COLLEGE CAMPUS AND GUVE THE MEASURES FOR ORDERLY PARKING OF VEHICLES	2

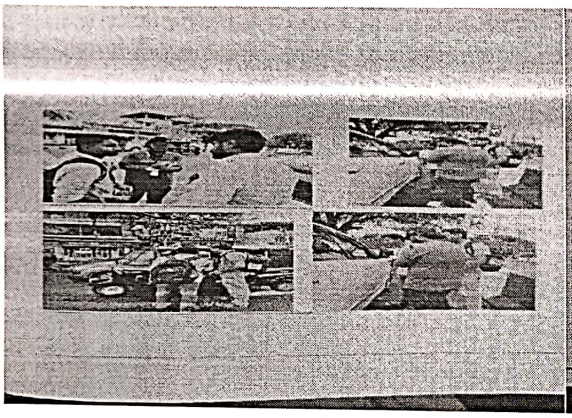

SPOT SPEED DATA
CONCLUSION:
Maximum number of vehicles are moving in the speed range of 70 80 KMPH

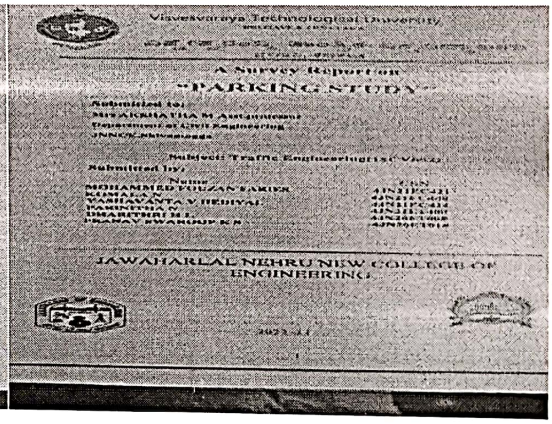

A SURVEY REPORT ON
TRAFFIC VOLUME COUNT
Date of Submission:
08 July 2023
Submitted to:
Akshatha Hills, M.tech
Dept. of Civil Engineering
JNNCE, Shimoga
Team Members:
Arjun C.M 4JN20CS013
Bheeranagouda 4JN20CS018
Kushal K. N 4JN20CS044
Mohammad Saheal 4JN20CS059
Shreya G 4JN20CS099
Surya S 4JN20CS108
Vijendra S N 4JN20CS118
Kshema T Byadagi 4JN21CS400
LOCATION OF SERVEY:
JNNCE 3rd GATE
BUS STAND

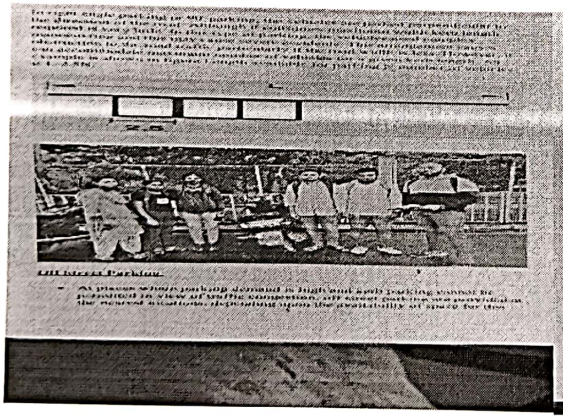

PCU VALUES GRAPH:
PCU/15 MIN (SHIMOGA TO SAVLANGA)
PCU/15 MIN (SAVLANGA TO SHIMOGA)
TIME
PCU
PHOTOS OF CS SURVEYING

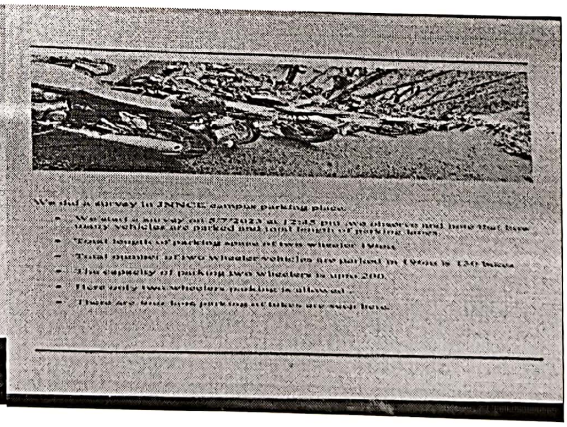












Mrs. Akshatha M
Assistant Professor
Course faculty

HOD CIVIL
Professor & Head
Department of Civil Engineering
J.N.N. College of Engineering,
Shimogga-577 204.

Department of Chemistry
Student Activity Report

Student Name

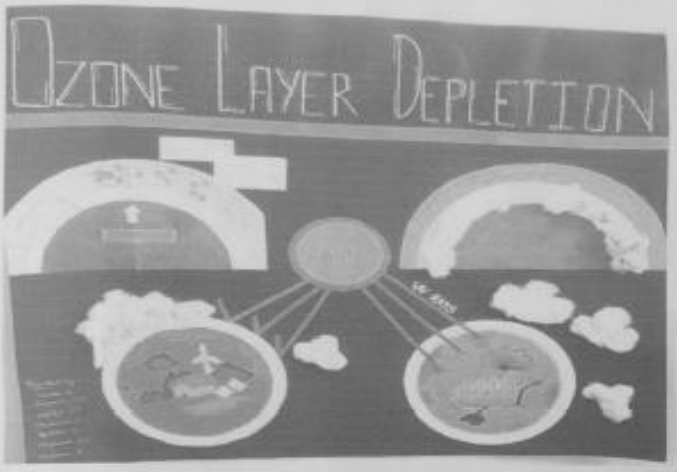
M Shanon Akanksha, Hajira Kouser

Student Team

Pooja B, Bhavana R M, Dhathri

Krishna V, Nisarga S

Student Activity on Research Based Programmes Tool Method (RBPT)
2020-21



Students Team

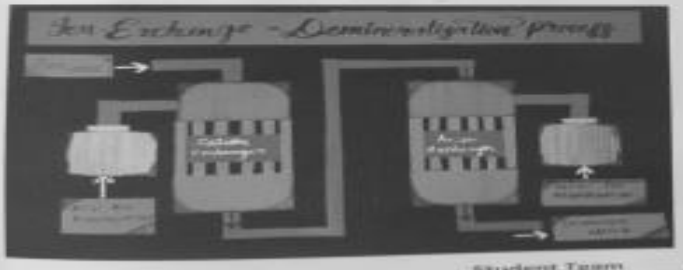
Likhitha R, Likhitha SR, Apeksha G, Madhura S, Meghana SN, Chaithra R, Priyanka H R

Student Team

Mahathi Kashyap, Jeevitha V, Amrutha VM, Rachana KP

Student Team

HM Hemanth Nayak, Ashish V Upadhya, B L Mallik, Hari BJ,
Hemanth CG, Pradeep, Amruthesh , Nikhil R nagar



Student Team

Angelina N, Prathaksha G, Gowri Hiremath, Avani adiga
Akshatha A P, Ganavi Patel, Inchara

Role Play

G.V. Sowmya

Computer Networks

https://www.youtube.com/watch?v=atMXCkjYh_k

Roleplay video on SMTP GV Sowmya

Roleplay

https://www.youtube.com/watch?v=fUXbNzmW7iI

Role play on Basics of Microprocessor

chethan gs
1 subscriber
Subscribe
2
Share

Roleplay

Mr. Girish Mantha

Data Communication (Computer Networks)

https://www.youtube.com/watch?v=e3Zn3qFYNZ4

Roleplay on OSI Reference Model

Girish Mantha Subscribe 7 Share Download

Flipped Classroom for the course: User Interface Design (20MCA254)
Handling Faculty: Dr. Hemanth Kumar

Students involved in flipped classroom activity where students are given a small topic prior and they discuss in the classroom.

J N N College of Engineering

Department of Computer Science & Engineering

Report on

SOFTWARE REQUIREMENTS SPECIFICATIONS ON E-COMMERCE SYSTEM

Submitted by,

POOJA.R	4JN20CS070
RUKMINI.S.	4JN20CS087
SHREYA.S.BHARADWAJ.	4JN20CS100
VARSHA.C.U.	4JN20CS115
YASHASWINI.I.K.	4JN20CS123

Table of Contents

3.2.2.1 Back-end Internal Computers
3.2.2.2 Internet Service Provider

3.2.3 **Performance**

3.2.4 **Security**

3.2.4.1 Data Transfer
3.2.4.2 Data Storage

3.2.5 **Supportability**

3.2.5.1 Configuration Management Tool

3.2.6 **Design Constraints**

3.2.6.1 Standard Development Tools
3.2.6.2 Web Based Product

Software Requirements Specification

1. Introduction

The Software Requirements Specification is designed to document and describe the agreement between the customer and the developer regarding the specification of the software product requested. Its primary purpose is to provide a clear and descriptive "statement of user requirements" that can be used as a reference in further development of the software system. This document is broken into a number of sections used to logically separate the software requirements into easily referenced parts.

This Software Requirements Specification aims to describe the Functionality, External Interfaces, Attributes and Design Constraints imposed on Implementation of the software system described throughout the rest of the document. Throughout the description of the software system, the language and terminology used should be unambiguous and consistent throughout the document.

1.1 Purpose

This document is meant to delineate the features of OSS, so as to serve as a guide to the developers on one hand and a software validation document for the prospective client on the other. The Online Shopping System (OSS) for web application is intended to provide complete solutions for vendors as well as customers through a single get way using the internet. It will enable vendors to set up online shops, and customer to browse through the shop and purchase them online without having to visit the shop physically. The administration module will enable a system administrator to approve and reject requests for new shops and maintain various lists of shop category.

In short, the purpose of this SRS document is to provide a detailed overview of our software product, its parameters and goals. This document describes the project's target audience and its user interface, hardware and software requirements. It defines how our client, team and audience see the product and its functionality. Nonetheless, it helps any designer and developer to assist in software delivery lifecycle (SDLC) processes.

1.2 Scope

This SRS is aimed at specifying requirements of software to be developed but it can also be applied to assist in the selection of in-house and commercial software products. The standard can be used to create software requirements specifications directly or can be used as a model for defining an organisation or project specific standard. It does not identify any specific method, nomenclature or tool for preparing an SRS.

3.1.1 Sell Configured to Ordered Products.

The system shall display all the products that can be configured.
The system shall allow the user to select the product to configure.
The system shall display all the available components of the product to configure
The system shall enable users to add one or more components to the configuration.
The system shall notify the user about any conflict in the current configuration.
The system shall allow users to update the configuration to resolve conflict in the current configuration.
The system shall allow users to confirm the completion of current configuration.

3.1.2 Provide comprehensive product details.

The system shall display detailed information of the selected products.
The system shall provide browsing options to see product details.

3.1.3 Detailed product Categorizations

The system shall display detailed product categorization to the user.

3.1.4 Provide Search facility

The system shall enable users to enter the search text on the screen.
The system shall enable users to select multiple options on the screen to search.
The system shall display all the matching products based on the search.
The system shall display only 10 matching results on the current screen.
The system shall enable users to navigate between the search results.
The system shall notify the user when no matching product is found on the search.

3.1.5 Maintain customer profile.

The system shall allow the user to create a profile and set his credential.
The system shall authenticate user credentials to view the profile.
The system shall allow user to update the profile information.

3.1.6 Provide personalized profile.

The system shall display both the active and completed order history in the customer profile.
The system shall allow user to select the order from the order history.
The system shall display the detailed information about the selected order.
The system shall display the most frequently searched items by the user in the profile.
The system shall allow the user to register for newsletters and surveys in the profile.

The system shall calculate tax for the order.
The system shall display tax information for the order.

3.1.14 Allow multiple payment methods.

The system shall display available payment methods for payment.

The system shall allow users to select the payment method for order.

3.1.15 Allow online change or cancellation of order.

The system shall display the orders that are eligible to change.
The system shall allow users to select the order to be changed.
The system shall allow users to cancel the order.
The system shall allow users to change shipping, payment methods.
The system shall notify the user about any changes made to the order.

3.1.16 Allow Online Product reviews and ratings.

The system shall display the reviews and ratings of each product, when it is selected.
The system shall enable the user to enter their reviews and ratings.

3.1.17 Offer financing options.

The system shall display all the available financing options.
The system shall allow users to select the financing option.
The system shall notify the user about the financing request.

3.1.18 Provide detailed sitemap.

The system shall allow users to view detailed sitemaps.

3.1.19 Offer online promotions and rewards.

The system shall display all the available promotions to the user.
The system shall allow users to select available promotions.

3.1.20 Online Purchase of products.

The system shall allow users to confirm the purchase.
The system shall enable users to enter the payment information.

The system shall not leave any cookies on the customer's computer containing any of the user's confidential information.

3.2.4.2 Data Storage

The customer's web browser shall never display a customer's password. It shall always be echoed with special characters representing typed characters.
The customer's web browser shall never display a customer's credit card number after retrieving from the database. It shall always be shown with just the last 4 digits of the credit card number.
The system's back-end servers shall never display a customer's password. The customer's password may be reset but never shown.
The system's back-end servers shall only be accessible to authenticated administrators.
The system's back-end databases shall be encrypted.

3.2.5 Supportability

3.2.5.1 Configuration Management Tool

The source code developed for this system shall be maintained in configuration management tools.

3.2.6 Design Constraints

3.2.6.1 Standard Development Tools

The system shall be built using a standard web page development tool that conforms to either IBM's CUA standards or Microsoft's GUI standards.

3.2.6.2 Web Based Product

There are no memory requirements. The computers must be equipped with web browsers such as Internet explorer. The product must be stored in such a way that allows the client easy access to it.
Response time for loading the product should take no longer than five minutes. A general knowledge of basic computer skills is required to use the product.

Department of Computer Science & Engineering
Pedagogical Initiative
2020-2021 (EVEN)

OPERATING SYSTEMS (18CS43)

Circular

The students are informed to see the specifications in your computer/laptop and write its specification. Also map it with concepts you learnt such as type of CPU, no. of cores, threads, cache, type of memory etc. Also compare your info with any other existing one and bring out the differences (ex: SDD and HDD etc). Submit the assignment per group with proper index sheet and group number and group members' name.

Sankhya N Nayak

INDEX

Sl no.	Date of Submission	Activity Na
1	27/06/22.	Personal (or

CACHE MEMORY :

Cache memory is a small-sized type of volatile computer memory that provides high-speed data access to a processor and stores frequently used computer programs, applications and data.

A temporary storage of memory, cache makes data retrieving easier and more efficient. It is the fastest memory in a computer, and is typically integrated onto the motherboard and directly embedded in the processor or main random access memory (RAM).

HARD DISK DESCRIPTION :

512GB SSD:

An SSD writes data up to 20 times faster and reads data upto 10 times faster than a mechanical HDD. It provides enough speed and storage to simultaneously load applications or play games

Available storage space : Provides about 400 GB.

OPERATING SYSTEM :

Windows 11 Home 64.

Windows 11 is the latest major release of Microsoft's windows NT operating system, released in October 2021. It is a free upgrade to its predecessor, windows 10, available for any windows 10 devices that meet the new windows 11 system requirement.

CORES IN PROCESSOR :

A core, or CPU core, is the "brain" of a CPU. It receives instructions, and performs calculations, or operations to satisfy those instructions. A CPU can have multiple cores. A processor with two cores is called a dual-core processor; with four cores, a quad-core; six cores, hexa-core; eight cores, octa-core.

THREADS IN PROCESSOR :

Threads are the virtual components or codes, which divides the physical core of a CPU into virtual multiple cores. A single CPU core can have up-to 2 threads per core.

28/06/22

Topic:-

Personal computer

Processor:- Intel(R) core(TM) i3 -2100 CPU @ 3.10 GHz.

Memory :- RAM - 4.00GB + 1TB hard disk.

Graphics:- NVIDIA Geforce GT 710

Primary hard disk:- (146GB Total)

Operating System:- X64 bit operating system.

CPU specifications:- Total cores 2, threads 4, Processor Base frequency 3.10 GHz.

*) Cache 3MB, Bus speed 5GT/s.

Q:- What is Processor Base frequency?

Ans:- It is the CPU's regular operating point. Max turbo frequency is the maximum speed of the CPU's operating point.

*) 3.1 billion times per second. It means processor work according to a clock that beats a set number of times per second. It can independently perform or process all computational tasks.

Q:- What are threads?

Ans:- A thread is a unit of execution on concurrent programming. These are virtual components or codes. A single CPU has 2 threads.

There are 4 threads.

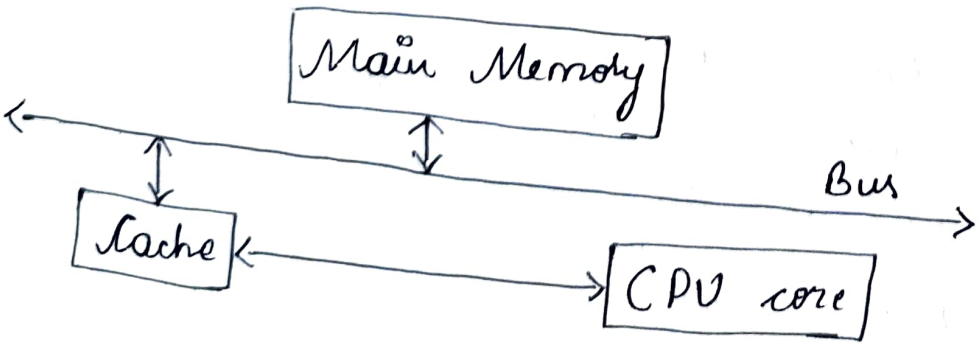
Cache Memory:-

A CPU cache is a hardware cache used by the central processing unit of a computer to reduce the average cost to access data from the main memory. It stores copies of the data from frequently used main memory locations.

PC has 3MB cache:- stores half the information of a system with a 6MB cache, the computer may need to go to a lower level cache to find the data it needs.

X64 bit operating system:-

An operating system that is designed to work in a computer that process a 64 bits at a time.



CPU cache.

Hardware

Product name : Ideapad Gaming 3 15IHU6

Processor :
Processor family : 11th Generation Intel Core™ i5 processor - 11300H
Speed - 3.1 GHz (Base) - 4.4 GHz (Max).
Cores - 4 cores.
Threads - 8
Cache - 8 MB.

Graphics :

NVIDIA GeForce GTX 1650 4GB GDDR6 dedicated graphic

Memory

RAM : 8GB (Upgradable upto 16 GB)
SSD : 512 GB

Operating System :

Windows 11 Home 64.

National Education Society (R.)
Jawaharlal Nehru National College of Engineering, Shivamogga
(Approved by AICTE, New Delhi, Certified by UGC 2f & 12B, Accredited by NAAC – 'B', UG programs: CE,ME,EEE,ECE,CSE,ISE,TCE acredited by NBA: 1.7.2019 to 30.6.2022,
Recognized by Govt. of Karnataka and Affiliated to VTU, Belagavi)

Department of Computer Science & Engineering
Pedagogical Initiative
2020-2021 (ODD)

PROBLEM SOLVING THROUGH PROGRAMMING (21PSP13)

Activity 1: Students were asked to write a program to generate electricity bill to understand the application of programming in real world.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Real world problem solving using group discussion. E.g., Electricity bill generation. etc.,
2. Demonstration of solution to a problem through programming.
3. Demonstration of simple project and motivating the students to develop similar type of projects.

With reference to the above suggested activity by VTU, the following exercise is to be carried out by students.

Calculate Electricity bill using Mescom format for Domestic Users in City

How do I calculate my electricity meter reading?

1. UNIT CONSUMED = CURRENT MONTH UNIT(KWH) – PREVUOUS MONTH UNIT(KWH)
2. ENERGY CHARGE (EC)= UNIT CONSUMED x UNIT RATE.
3. FIXED CHARGE (FC)= SANCTION LOAD x FIXED CHARGE RATE.
4. ELECTRICITY DUTY (ED)= (ENERGY CHARGE + FIXED CHAREG)x TAX RATE/100.
5. TOTAL ELECTRICITY BILL= ENERGY CHARGE+ FIXED CHARGE+ ELECTRICITY DUTY.

Assume Fixed charge as Rs. 200

How is electricity bill calculated in Mangalore?

Karnataka electricity board single slaps for the domestic LT supply such as for 0 to 30 units the per-unit cost will be ₹ 3.75/-, from 31 to 100 the per-unit cost will be ₹ 5.20, from 101 to 200, the per-unit cost will **be ₹ 6.75** and above 201 units you have to pay ₹ 7.8 per unit.

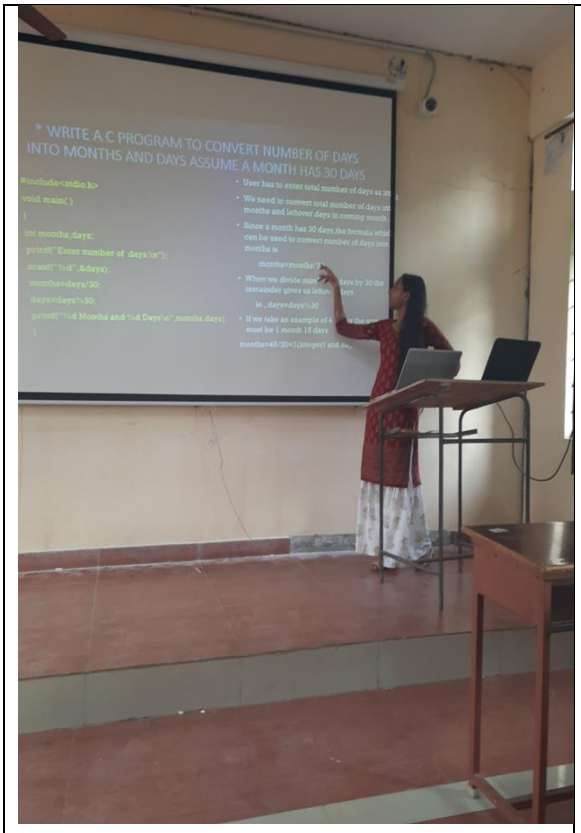
What is electricity levied tax?
Application of Electricity Duty or Tax

State	Domestic	Commercial
Karnataka	6%	6%
Kerala	10%	10%
Madhya Pradesh	9-15%	9-15%
Maharashtra	15%	17%

Activity 2: After the syllabus was completed, students were given topics of their choice to study, prepare presentation and give examples other than the one available in their textbook.

Images of presentation available at : https://drive.google.com/drive/folders/1RLD6V6-i2F1dQeMboVCYN5ZkGLbZGol0?usp=sharing

USN	NAME	Q.No	USN	NAME	Q.No
4JN21CV002	ABHISHEK N K	1 a	4JN21EE035	SINCHANA M	19 a
4JN21CV006	AMITH S	1 b	4JN21EE037	SUDEEP G J	19 b
4JN21CV022	DIVYA N S	2 a	4JN21ET006	BHAVANA V	20 a
4JN21CV031	HUTTHESH KUMAR M P	2 b	4JN21ET013	FOUZIYA BANU	20 b
4JN21CV039	NANDISH K S	3 a	4JN21ET026	PALLAVI N R	21 a
4JN21CV052	SAHANA L	3 b	4JN21ET033	PRUTHWI D B	21 b
4JN21CV054	SAMARTH B R	4 a	4JN21ET040	SANJAYA S	22 a
4JN21EC001	ABHIJNAA S N	4 b	4JN21ET041	SHREENANDA S	22 b
4JN21EC008	AMITH H B	5 a	4JN21ET046	SYED INSHAAZ	23 a
4JN21EC009	AMRUTHA K B	5 b	4JN21ET048	UJWAL D H	23 b
4JN21EC010	AMULYA M	6 a	4JN21ET051	VARSHA T	24 a
4JN21EC011	ANANYA S K	6 b	4JN21IS014	ANVITHA V	24 b
4JN21EC014	ARUN MANJAPPA B	7 a	4JN21IS015	ASHITHA D	25 a
4JN21EC017	BHARATH V M	7 b	4JN21IS016	B AMAN ULLA	25 b
4JN21EC018	BHAVYASHRI SHRIPAD D	8 a	4JN21IS027	GURUKIRAN B	26 a
4JN21EC021	CHETAN GURUMATH	8 b	4JN21IS038	JAHNAVI O M	26 b
4JN21EC026	DEEKSHITH H S	9 a	4JN21IS049	MADHUSUDAN S	27 a
4JN21EC027	DEEPALI C	9 b	4JN21IS050	MANASA K	27 b
4JN21EC035	JEEVAN P	10 a	4JN21IS062	NESARA K U	28 a
4JN21EC038	K BHASKAR	10 b	4JN21IS065	NITHISH A S	28 b
4JN21EC043	KESHAV S SINDHE	11 a	4JN21IS067	PAVAN KUMAR	29 a
4JN21EC045	L K SINDHU	11 b	4JN21IS080	RITHISH K R	29 b
4JN21EC053	MAHEEN TABISH	12 a	4JN21IS094	SHREYA A P	30 a
4JN21EC066	PRAGATI SURESH NAIK	12 b	4JN21IS108	SUCHIN N H	30 b
4JN21EC067	PRAJWAL G M	13 a	4JN21IS111	SUSHMITHA H S	31 a
4JN21EC076	RAHUL N	13 b	4JN21IS112	SUSHMITHA S S	31 b
4JN21EC084	S ANUSHA	14 a	4JN21IS117	TEJASWINI N R	32 a
4JN21EC092	SINDHU H B	14 b	4JN21ME003	AREEB IMTIAZ AHAMED	32 b
4JN21EC093	SUJITH B N	15 a			
4JN21EC095	SUSHANTH G RAO	15 b			
4JN21EC104	VEDAVATHI G N	16 a			
4JN21EE010	DARSHAN D	16 b			
4JN21EE014	HARINI K M	17 a			
4JN21EE022	NAVANA G N	17 b			
4JN21EE026	POOJA S GODI	18 a			
4JN21EE033	RAKSHITHA Y C	18 b			


WRITE A C PROGRAM TO CONVERT NUMBER OF DAYS INTO MONTHS AND DAYS ASSUME A MONTH HAS 30 DAYS
#include<stdio.h>
void main()
{
int months,days;
printf("Enter number of days:\n");
scanf("%d",&days);
months=days/30;
days=days%30;
printf("%d Months and %d Days\n",months,days);
}
User has to enter total number of days as in
We need to convert total number of days in
months and leftover days in coming month
Since a month has 30 days,the formula which
can be used to convert number of days into
months is
months=months/
When we divide num days by 30 the
remainder gives us leftov days
ie., days=days%30
If we take an example of
must be 1 month 15 days
months=45/30=1(integer) and da..


FORMATTED INPUT/OUTPUT
FORMATTED INPUT:


DATATYPE HIERARCHY
int
Unsigned int
long
Unsigned long
Long long
Unsigned long long
float
double


Simple Calculator Program Using Switch Statement
{C}
PROGRAMMING
Name: Samarth BR
Sem:1
Section:G

Seminar activity for 1st year B.E students

Electrochemical theory of Corrosion

Department of Chemistry, JNNCE, Shimoga

Seminar Activity for I year student 2021-22.

Rakshitha
Apoorva.
Nithyashree.
Arundathi. T.S
Bhoomika. E
Lakshmi. U.S
Dakshayini.

Video Lecture Assignment

Dr. Ashwini S. R. • Oct 16, 2019

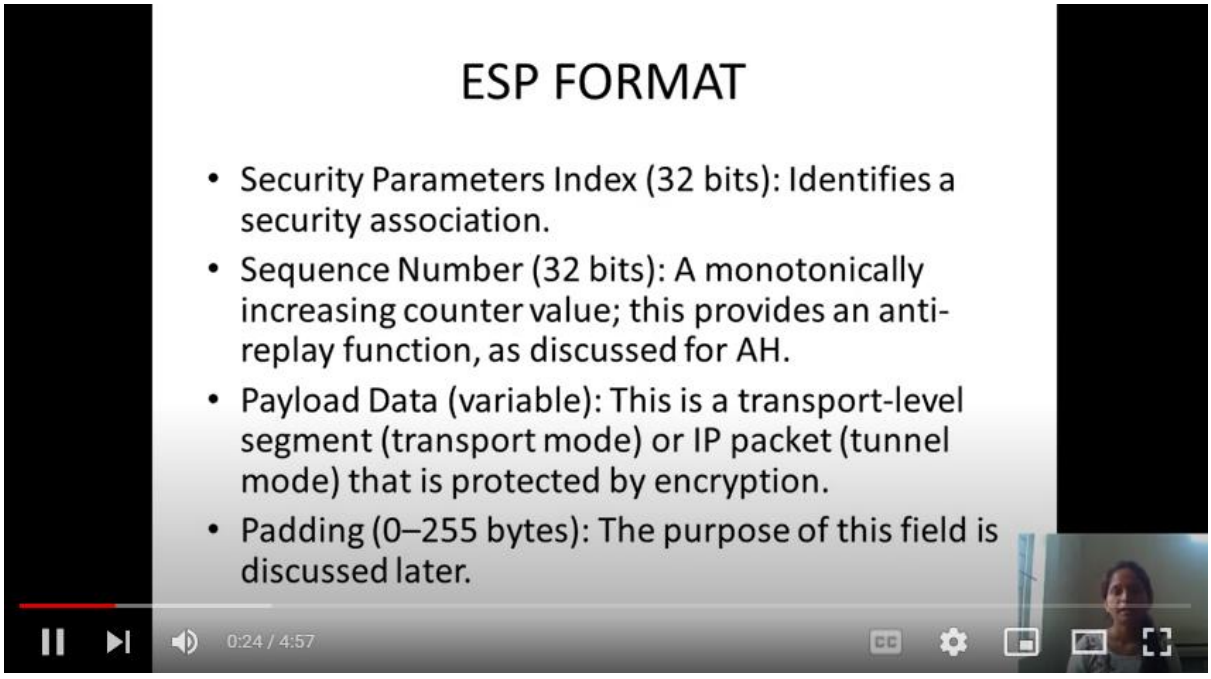
2 points | Due Oct 21, 2019

1. Make a batch of 3/4 students (Project batch should work well)
2. Create a video of 2 mins each on the topic given in the list below
3. Stitch the videos as per the batch and topic
4. Upload the video to YouTube and post the link on this classroom.

Topics:
1. Pretty Good Privacy
2. S/MIME
3. IP Security Overview & IP Security Policy
4. Encapsulating Security Payload
5. Combing Security Associations
6. Internet Key Exchange
7. Cryptographic suites

Hint: Refer Text book "Cryptography & Network Security", William Stallings.

Available at : https://www.youtube.com/watch?v=XtON6TV8lU0



Vishweshwarayya Technological University

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ

ಬೆಳಗಾವಿ, ಕರ್ನಾಟಕ

OPERATING SYSTEM

Activity Report on

Activity-2 Unix Operating system

Submitted by :

GROUP NO.5

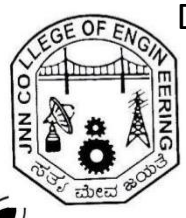
Under the guidance of

Mrs. JOYTHI.K

Professor.

Dept. of IS & E,

JNNCE, Shivamogga



Department of Information Science & Engineering

J N N College of Engineering

Shivamogga - 577 204

SUBMITTED BY:

(1)NAME:NIDEEP G.P –USN:4JN19IS055

(2) NAME:NIKHIL J.S-USN:4JN19IS056

(3) NAME:NISCHAL A.G-USN:4JN19IS057

(4) NAME:NISCHITHA G.S-USN:4JN19IS058

(5) NAME:BHOOMIKA H.P- USN:4JN20IS401

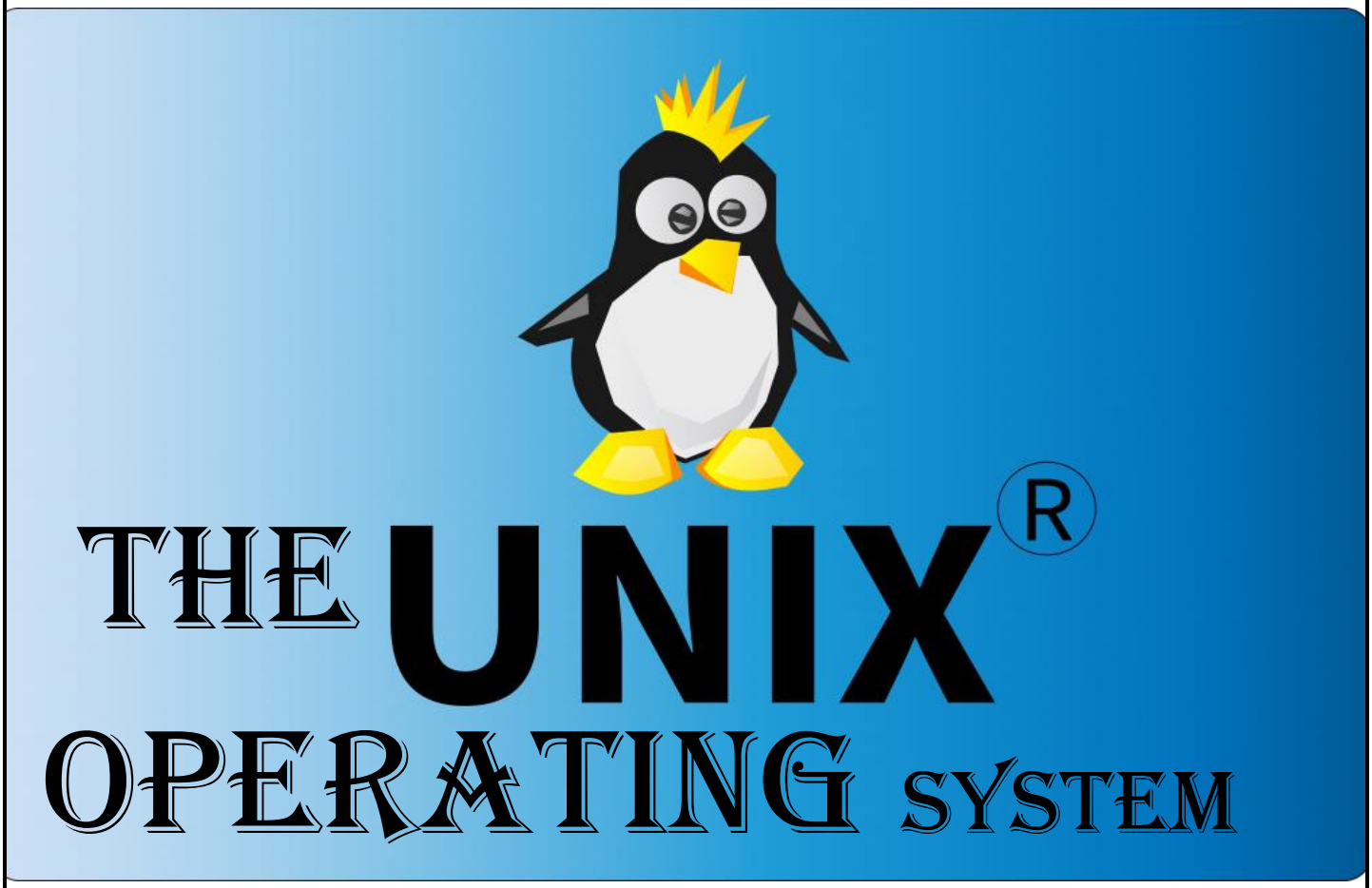
(6) NAME:PRATHIKSHA G- USN:4JN20IS404

(7) NAME:SANJANA B.L-USN:4JN19IS405

(8) NAME:SATHWIK PAI-USN:4JN19IS406

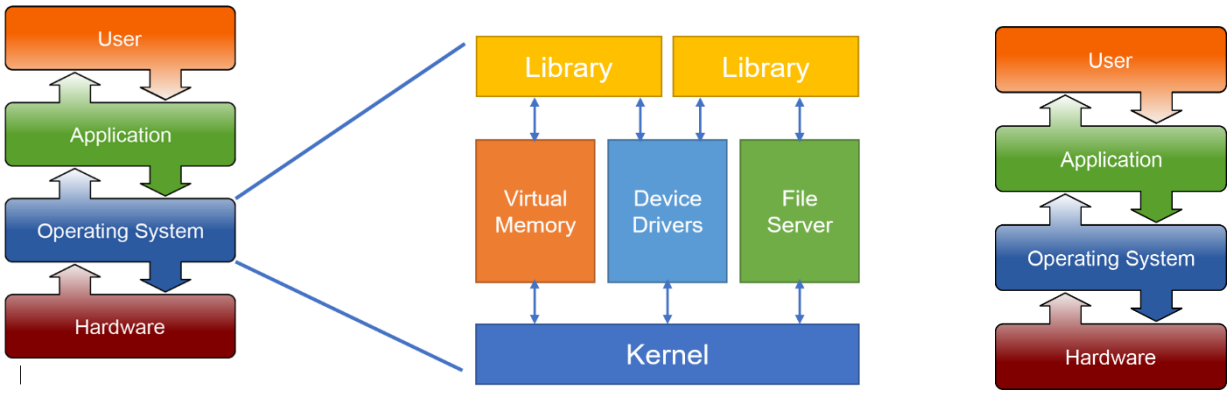
(9) NAME:SOUNDARYA.P-USN:4JN19IS408

(10) NAME:VISMAYA N.U-USN:4JN19IS409


THE UNIX®
OPERATING SYSTEM

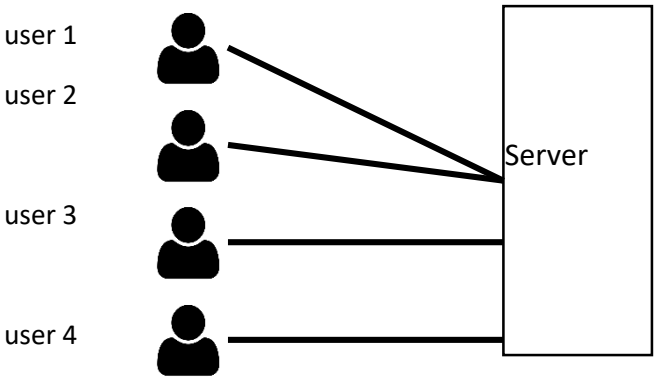
Operating Systems:

- Operating systems allow the separation of hardware management from applications/programs.
- This allows the applications to work across different hardware platforms, although the applications are still specific to the OS.



- The Kernel is the core function of the OS and handles basic-level communication between the various processes and the hardware.
- Libraries provide applications with standardized access to kernel functions.

Client/Server architecture:



TERMINOLOGY:

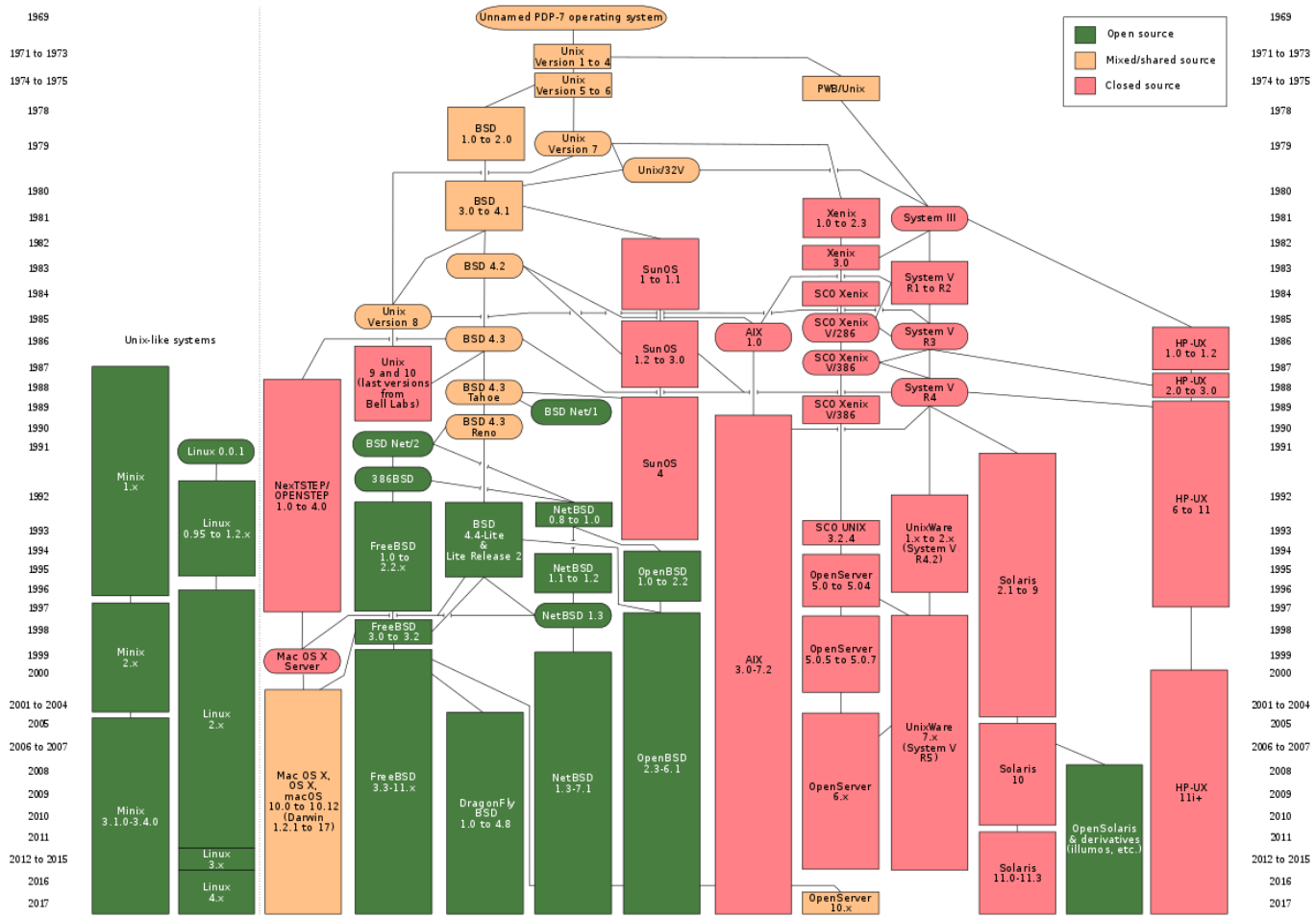
Terminal: Device or Program used to establish a connection to the UNIX server

- Shell: Program that runs on the server and interprets the commands from the terminal.
- Command line: The text-interface you use to interact with the shell.

UNIX operating system:

- First developed in 1970s, it is a multitasking OS that supports simultaneous use by multiple users.
- Strengths
- Command-line based.
- Supports thousands of small programs running simultaneously.
- Easy to create pipelines from individual programs.
- Multi-user support and partitioning is baked in.
- Challenges
- Command-line based.
- Finding help and documentation can be onerous.
- Many different variants

UNIX and its derivatives



Application Programming Interface (API)

- Biggest strength is the ability to connect different programs together.
- Programs/Applications need to be able to communicate.
- A pre-defined set of methods to communicate with an application is called it's API.
- Each program comes with its own API.

Programs vs. libraries:

- Programs/Applications: Perform a defined task that accepts one or more inputs and produces an output.
- Example: ls – lists contents of current location.
- Libraries: Collection of related functions that may be used by different programs.
- Example: GNU Scientific library – provides a set of complex math functions
- Users typically interact with programs, while programmers use libraries within their code.
- Both Programs and Libraries have APIs.

POSIX standards:

- Standards defined by IEEE computer society to maintain portability between different UNIX OS's.
- Originally defined standard API for core processes eg., kernel level access.
- Later expanded to include programs and utilities used directly by the user.
- Net result: Common UNIX commands you learn will be usable across UNIX/ Linux/MacOS etc.
- UNIX and MacOS (version 10.5 and above) are POSIX-certified

GNU/Linux OS:

- Most Unix-like operating systems are a variant of this scheme.
- Linux is typically the kernel of this OS.
- The rest of the utilities/applications were derived from the GNU project.
- Vast majority of commands you will type fall into the GNU portion of the OS.

- This user-interfacing part of the OS is often called User space.
- GNU/Linux is POSIX-compliant i.e., it mostly follows POSIX with a few exceptions

User vs. Kernel space:

- User space: Set of applications/utilities that interact with the user. Also includes, the portions of the file system where these files reside AND the portion of memory (RAM) where the programs are loaded and run.

- Kernel space: Set of applications that form middle layer between hardware and user applications. These program operate in a separate, protected portion of the RAM.

UNIX file system:

- All UNIX files, including system and user files reside in a hierarchical directory structure.
- The file system maintains the record of where each file resides on the hardware.

- The lowest level or base of this structure is called the ‘root’ directory represented as /
- Every user has a defined home directory
- My home is: /home/kvarala

Files and Directories:

- Files are the basic unit of storage. Eg., This presentation file.
- Directories are containers that hold sets of related files. Eg., Set of presentations for this course.
- Each file name within a directory has to be unique.
- UNIX is case-sensitive i.e., the file example.txt is different from the file Example.txt
- Directory names are also case-sensitive

Files contd..

- File extensions eg., .txt or .jpg or .doc etc. have no relevance in UNIX.
- It is good practice for users to use a file extension that describes the file type.
- Use long descriptive names for your files. File name length is allowed up to 255 characters.
- File size limits are defined by the file system used by the OS.
- Current file systems support file sizes larger than the capacity of current hardware (2^63 bytes).

Typical structure of UNIX:

/bin ==> Programs/Utilities. Typically OS files.

/etc ==> Administrative files. Usually, OS related.

/home ==> Home directories of users.

/lib ==> Libraries. OS or installed software.

/mnt ==> Mounted devices. Eg., CD/DVD, USB drive.

/root ==> Home for root/administrative user.

/tmp ==> Temporary files. OS, software and user.

/usr ==> User-space programs/Utilities

/var ==> System generated temporary files.

File paths:

- In a shell you are always in a particular location.

Default location after login is your home

- Eg: /home/kvarala
- Every file has a location on the server.
- Path defines the location of the file/directory.
- Path can be defined two ways:
- Absolute: Path starts from Root. Eg.,

/scratch/scholar/k/kvarala/Week1/Lecture_1.pdf

- Relative: Path starts from current location. Eg.,

../Week2/Lecture_2.pdf

- Special characters:
- . Means current directory
- .. Means parent directory
- ~ Means home directory

Command line:

- Every word you type in the command line is interpreted by the shell as a command.
- If the shell cannot interpret the command it returns the error: “command not found”.
- The shell looks for the program matching the typed command in the locations defined by PATH.
- User can add commands by adding programs to their PATH.

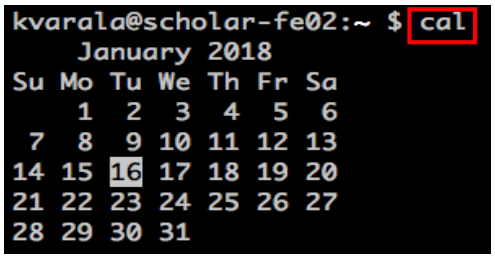
I/O streams:

- Each command has 3 Input/Output streams:
- STDIN : Standard Input is the default stream that inputs data into a command. Example: keyboard, file etc.
- STDOUT : Standard Output is the default output stream of the command. Example: Terminal
- STDERR: Standard Error is where the errors from the program are displayed:

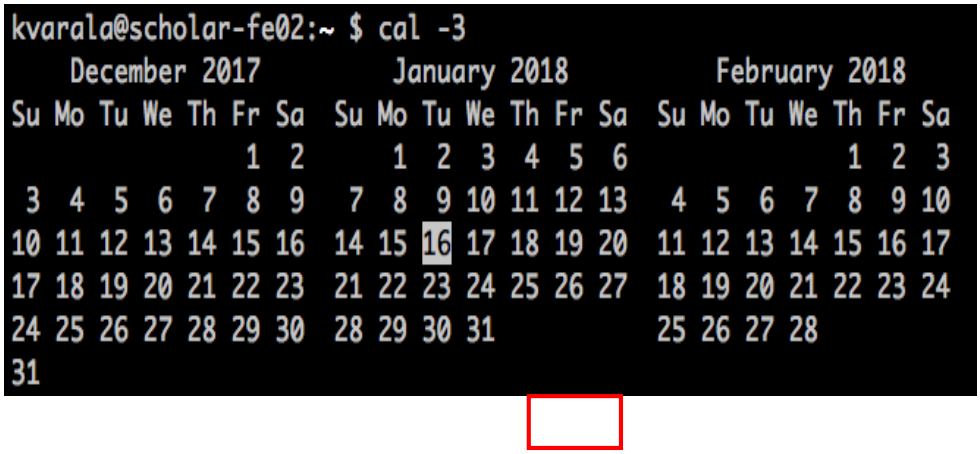
Example: Terminal

Anatomy of a command:

- Let's explore commands with a easy command called cal:
- This command by default displays the calendar for this month with today highlighted.



- Commands can often take arguments, which change the default settings.
- The argument -3 changes display to 3 months with current month in the center.



Example UNIX commands:

- ls stands for list. This command lists the contents of the current location.
- pwd stands for print working directory. This command tells you your current location in the shell.
- hostname gives you the name of the host that the shell resides on.
- who lists all the users currently logged into the server.

Let's explore ls:

- ls is a basic but powerful command.
- It has over 50 arguments to alter its behavior.
- The most commonly used one is the 'long list format' specified by the switch -l .
- Try typing in ls in your scratch folder:
- Now, try typing in ls –l

Metadata on files and directories

- Metadata is information about the file that are not part of the contents of the file.
- Three main parts to it:
- Ownership and access permissions
- Size
- Timestamp

UNIX permissions:

- Execute == 1
- Write == 2
- Read == 4

Common Permission settings	Indicator	Numeric code
Read-only	r--	4
Read & execute	r-x	5
Read & write	rw-	6
Read, write, execute	rwx	7

UNIX permissions:

```
kvarala@scholar-fe02:/scratch/scholar/k/kvarala $ ls -l
total 232
-rw-r--r-- 1 kvarala student 227905 May  5  2017 rcac_cluster_reference.pdf
drwxr-xr-x 2 kvarala student   4096 Jan 16 12:02 Week1
drwxr-xr-x 2 kvarala student   4096 Jan 16 12:02 Week2
```

Permissions

- First character is - for a file and d for a directory.
- Characters 2-4 refer to permissions the owner sets for himself.
- Characters 5-7 are permissions for the group listed.
- Characters 8-10 are permissions for the world (i.e., every other user)

Permission settings	Indicator	Numeric code
Read-only	r--	4
Read & execute	r-x	5
Read & write	rw-	6
Read, write, execute	rwx	7

Working with directories:

- pwd -> lists the present working directory
- mkdir -> makes a new directory
- cd -> change directory
- rmdir -> remove directory
- Try using cd with path:
- cd /scratch/scholar/k/kvarala
- cd ./Week1
- cd ../Week2

File commands:

- mv is the move command that moves a file. This command is also used for renaming files.
- rm is the remove command and will remove the file or empty directory listed as argument.
- cat is the catenate command that joins the contents of all files given as arguments.

Creating pipelines from commands:

- The STDIN and STDOUT of each command can be redirected to combine programs together.
- For example, the STDOUT of one program can be sent to the STDIN of another program.
- We will go over examples in tomorrow's lab section

Summary:

- UNIX is a text-based, multiuser OS, that supports simultaneous execution of thousands of commands.
- UNIX is case-sensitive for file names and command names.
- Each command is a program stored as a file in specified location.
- Commands can be combined by redirecting I/O streams.
- Each file has a path that uniquely identifies its location.
- Access to files and directories is controlled via permissions set by the owner of the file.

Evaluating the classical UNIX scheduling

• Pros

+ simple and efficient

+ suitable for general-purpose time-sharing systems

+ avoids starvation

+ supports processes with I/O operations

• Cons

– does not scale well

– no guarantee for processes

– users can not configure scheduling (except for nice)

– no support for multi-processor, multi-core systems

– kernel mode is non-preemptive: A process running in kernel mode for a long time can hold up the entire system (priority inversion)

Modern UNIX schedulers (requirements)

• New scheduling classes

– special application needs (multimedia, real-time, etc.) – „fair share”: it is possible to plan the resource allocation

– multitasking at kernel level

– modular scheduling with and extendable framework • Kernel preemption – it is necessary for multiprocessor scheduling

• Performance, overhead

– scheduling became more and more complex (requirements, hardware)

– scheduling algorithms should scale well

• Threads or processes?

– modern applications use threads a lot (e.g. Java)

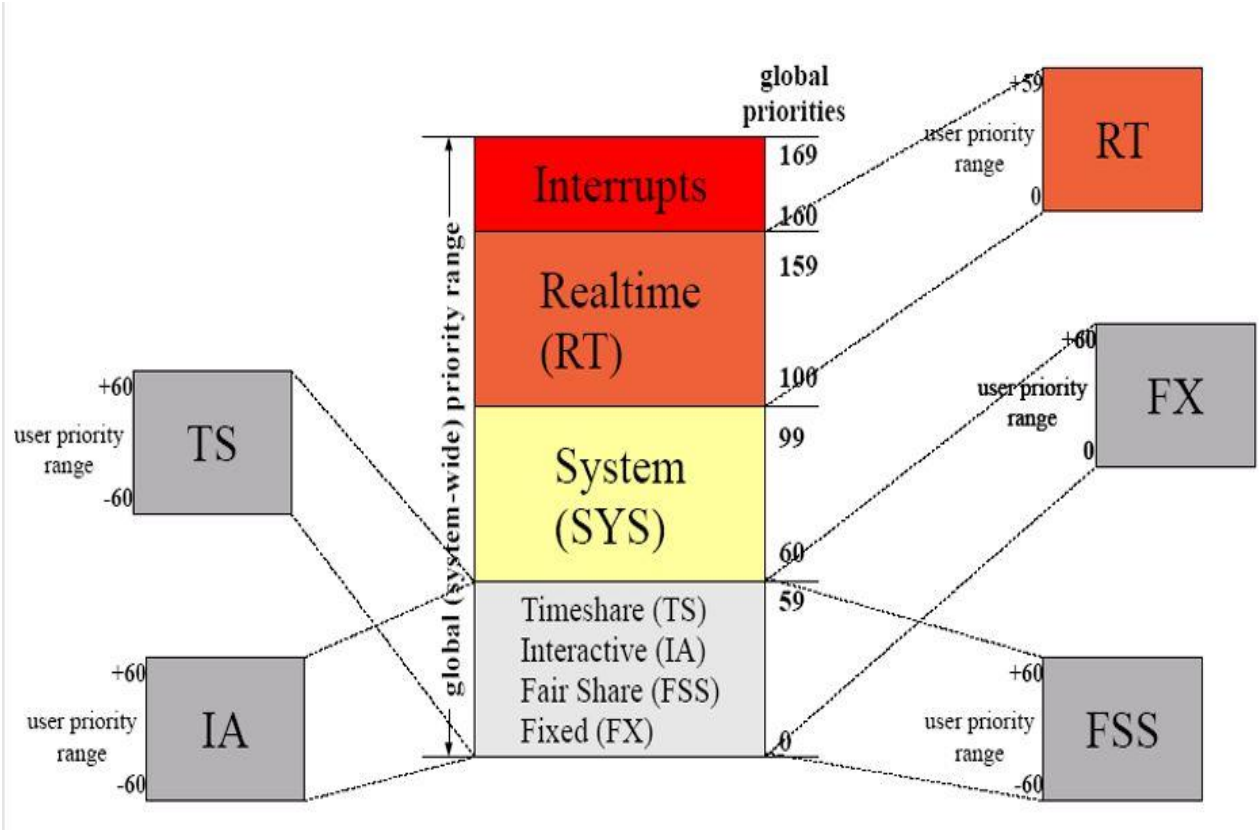
– schedulers should focus on threads not on processes

Scheduling in the Solaris operating system

• Characteristics
– scheduling is thread-based
– the kernel is fully preemptible
– supports multi-processor systems and virtualization
• New scheduling classes
– Time Sharing (TS): similar to the classical scheduling
– Interactive (IA): same as above but puts more emphasis on the active window on the graphical user interface
– Fixed priority (FX)

– Fair share (FSS): allocating CPU resources to process groups
– Real-time (RT): provides the shortest resonse time
– Kernel threads (SYS)

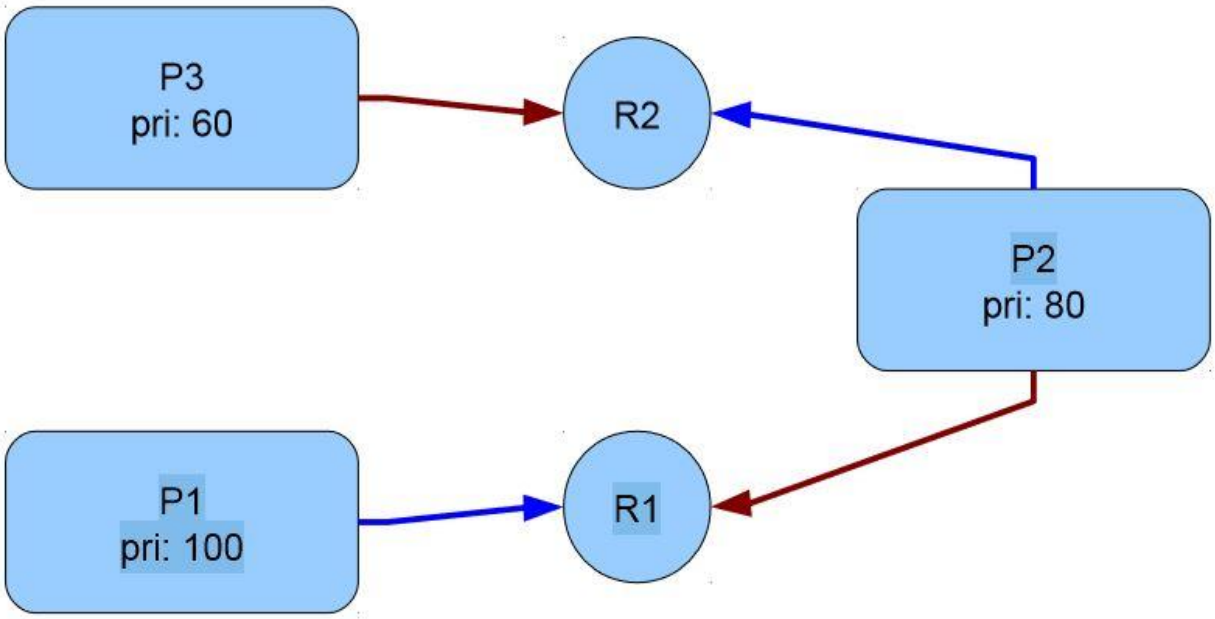
Solaris scheduling levels



Inherited priorities (Solaris)

• The problem of priority inversion (blue: waiting, red: holding)

• Solution: increasing the priorities according to the waiting scheme.



Linux schedulers

• Before kernel V2: based on the classical UNIX scheduler

• Before V 2.4

– scheduling classes: real-time, non-preemptive, normal – scheduling algorithm with O(N) complexity

– single runnable queue (no SMP support)

– non-preemptive kernel • Kernel v2.6 (Ingo Molnár)

– O(1) scheduler (scales very well)

– multiple runnable queues (better SMP support)

– a heuristic algorithm to differentiate between I/O and CPU-bound tasks

• comparing running and waiting (sleeping) times (takes considerable time)
• prefers I/O-bound processes
• 2.6.23 kernel: CFS (Completely Fair Scheduler)
– designed and implemented by Ingo Molnár, some ideas from Con Kolivas
– a new data structure for runnable processes: self-balancing red-black tree
– tries to be fair by calculating a „virtual" runtime for all processes

Linux scheduling information (practice)

• Acquiring information using the
/proc filesystem /proc/cpuinfo – available CPUs
/proc/stat – CPU and scheduler properties
/proc/loadavg – average system load (past 1, 5, 15 minutes)
/proc/sys/kernel/sched* – scheduler information
/proc/<PID>/status – process state, Cpus_allowed, ... /proc/<PID>/sched – process scheduling data

• What is happening on my computer?

– Interesting story: Peeking into Linux kernel-land using /proc filesystem Uses ps, strace, /proc/PID/... to debug a database problem
– Other interesting things to know: What Your Computer Does While You Wait

Linux CFS

• It replaces the previous O(1) scheduler with an O(log n) algorithm
• It uses a self-balancing red-black tree instead of simple linked lists
– this is a binary tree with O(log n) complexity search
– lower values to the left, higher to the right
– insert and delete is more simple
• Calculating the priority is based on
– number of virtually running processes (nr_running)
– virtual run time (vruntime) in the rbtree index

• Basic operations:

– enqueue_task: New task arrived (nr_running++)
– dequeue_task: Task no longer ready to run (nr_running--)
– pick_next_task: who is the next to run

UNIX CRON and AT: long term scheduling
• Executing tasks at given time(s)
– e.g. simple backup, maintenance tasks, etc.
• Usage
– AT: execute a task at a given time (at now + 1 day)
– CRON: periodically execute a task (see man crontab) minute, hour, day of month, month, day of week 0 6 * 1-6,9-12 2 /local/bin/lets_play_soccer Send an invitation every Tuesday morning at 6am (except during summer) */20 * * * * /local/bin/clear_old_temp_cache Clear temporary and cache files in every 20 minutes
• This scheduling is not performed by the kernel
– It is part of the user space program set.
– It starts certain tasks but does not govern them while they are running.
– After started these tasks belong to short term scheduling.

UNIX Memory Management

Memory is an important resource in computer. Memory management is the process of managing the computer memory which consists of primary memory and secondary memory. The goal for memory management is to keep track of which parts of memory are in use and which parts are not in use, to allocate memory to processes when they need it and de-allocate it when they are done. UNIX memory management scheme includes swapping and demand paging.

Memory Partitioning

The simplest form of memory management is splitting up the main memory into multiple logical spaces called partition. Each partition is used for separate program.

There are 2 types of memory partitioning

- Single Partition Allocation
- Multiple Partition Allocation

Single Partition Allocation:

Single partition allocation only separates the main memory into operating system and one user process area. Operating system will not able to have virtual memory using single partition. Using single partition is very ineffective because it only allows one process to run in the memory at one time.

Multiple Partition Allocation

Most of the operating system nowadays is using multiple partitions because it is more flexible. Multiple partition allocation enabled multiple programs run in the main memory at once. Each partition is used for one process.

There are two different forms of multiple partition allocation, which is fixed partitioning and variable partitioning. Fixed partitioning divides memory up into many fixed partitions which cannot be change. However, variable partitioning is more flexible because the partitions vary dynamically in the later as processes come and go. Variable partitioning (Variable memory) has been used in UNIX.

UNIX Memory Management Strategies

Program will be place into memory during execution. However, a large program will divide into small pieces and loading the pieces as they needed. Overlays will replace the new pieces with the program which is unused. UNIX is using this technique to run a new program by fork the running process which is also

known as fork-exec. The overlays technique is illustrated below.

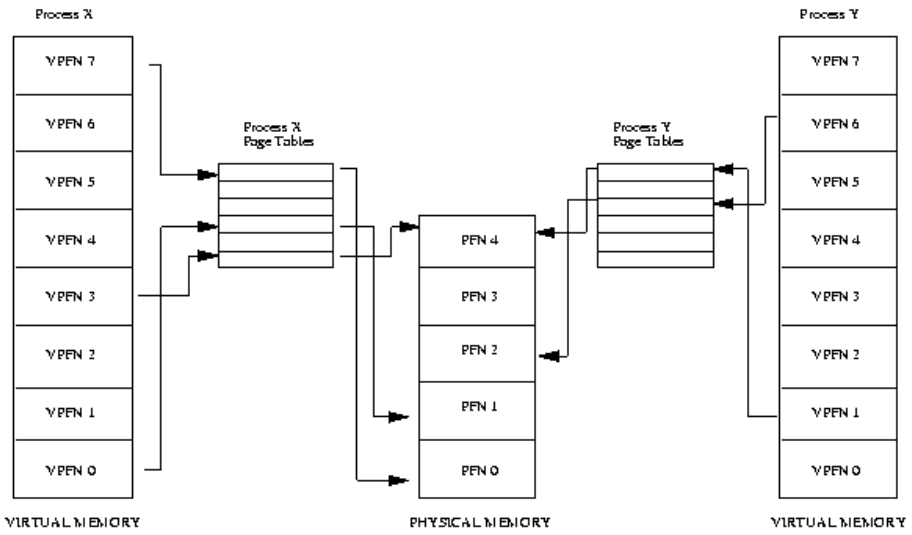
Swapping

Swapping consists of bringing in each process in physical memory entirely and running it. When the process is no longer in use, the process will be terminated or is swapped out to disk.

Initially only process A is in memory. Then process B is swapped into memory from disk. After that, process A terminates or swapped out to disk. Then process C is swapped into the free space.

External Fragmentation Problem

The size of each process is different, therefore when the processes is been swapped in and out, there will be a multiple holes in the memory because UNIX is using variable partitioning.



Solution

There are two techniques to solve this problem, which are memory compaction and fit in the process using algorithms

Compaction

Memory compaction moves all the processes upward as far as possible, so that all the free memory is placed in one large block. However, it is not a good idea because it requires a lots of CPU time.

Most processes will grow as they run, and the processes data segments can grow, as in many programming languages, the process will grow. If there is a hole is next to the process, it can be allocated and the process is allowed to grow into the hole. Therefore it is good to allocate some extra memory whenever a process is swapped in or out.

Algorithms

There are three different types of algorithm can be used to loads the program wherever the memory space is unused, which is first fit, best fit and worst fit.

Algorithms

Descriptions

First Fit

The memory manager scans along the list and allocates the first space to fit the process. First fit is a fast algorithm because it searches as little as possible.

Best Fit

The memory manager scans the whole list and takes the smallest hole that will fit the process. Best fit is slower than first fit because it must search the whole list every time it is called.

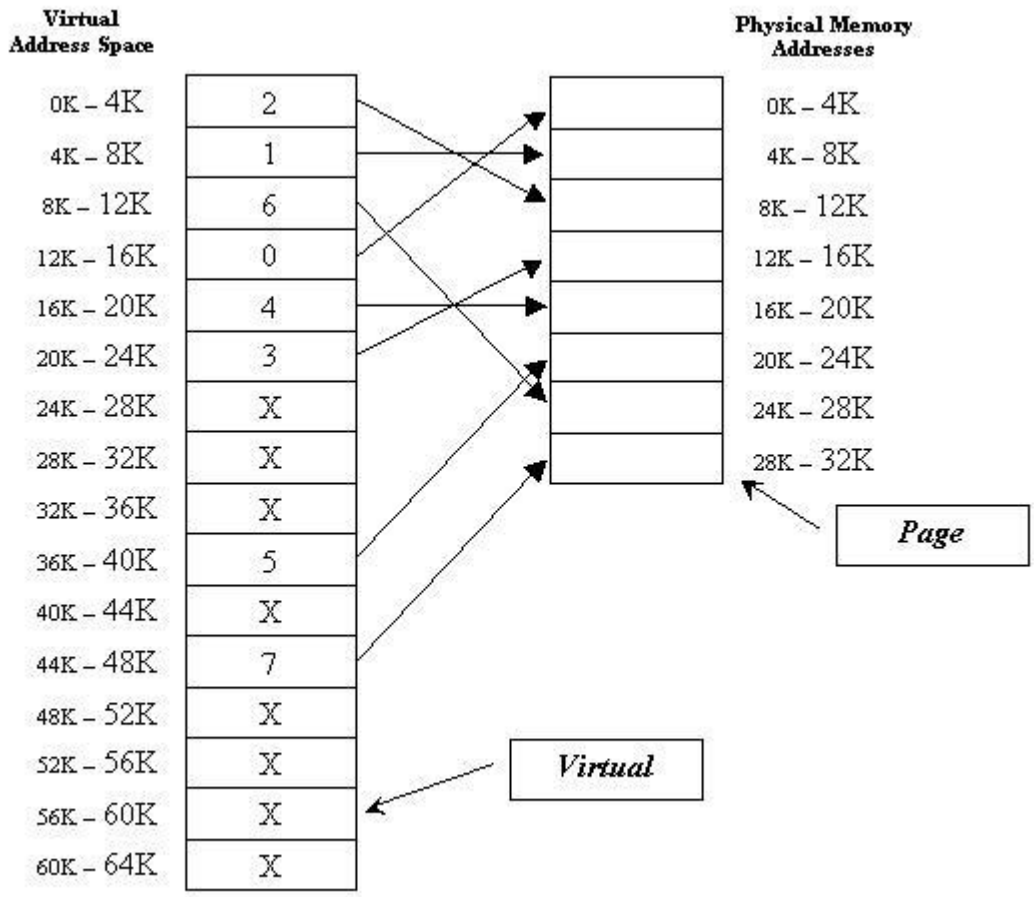
Worst Fit

The memory manager scans the whole list and takes the largest available hole, so that the hole broken will be big enough to be useful.

Virtual Memory

UNIX operating system allows user to fully utilize the physical memory installed in the system as well as part of the hard disk called swap space which have been designated for use by the kernel while the physical memory is insufficient to handle the tasks.

Virtual memory managers will create a virtual address space in secondary memory (hard disk) and it will determine the part of address space to be loaded into physical memory at any given time. The benefit of virtual memory relies on separation of logical and physical memory.



Demand Paging

Paging is a memory allocation strategy by transferring a fixed-sized unit of the virtual address space called virtual page whenever the page is needed to execute a program. As the size of frames and pages are the same, any logical page can be placed in any physical frame of memory.

Every processes will be logical divided and allocate in the virtual address space. There is a page table in the virtual memory to allocate and keep tracking of the pages to map into the frames.

Page Fault Problem

A page fault occurs when a program try to use a page that is not in the memory, due to demand paging will only paged the pages into the memory when it is needed. For example in figure 1.9, if the program try to use Page 1 for Process A in memory, the operating system will interrupt occurs as a result of trying access a missing page because Page 1 is not paged in the memory.

Solution for Page Fault

The steps in handling page fault. When page fault occurs during program execution, the kernel will first locate the missing page on the backing store (disk). After located the page, it will find a free memory frame in the physical memory and copy into it. The page table will be reset after that and the instruction will be restart.

Problem- No Free Frames

When all the frames in the memory is been used, the other problem will occurs. This will cause the pages is unable to paged into the memory.

Solution- Page Replacement Algorithms

Solution for no free frames problem is to find a memory frame that is idle and free the frame using a page replacement algorithm. There are three common types of page replacement algorithm such as First in First out (FIFO), Optimal and Least Recently Used (LRU).

UNIX is using least recently used algorithm for page replacement. The least recently used algorithm replaces the page that has not been used for the longest time, on the assumption that the page will not be needed again. The page table will record every time the page being referenced, and when page replacement is needed, every page will be checked to find the oldest recorded time.

Conclusion

Every operating system has different memory management. UNIX also has their exclusive memory management strategies to manage the memory resource optimally. UNIX is using multiple and variable partitioning so that the memory can be stored and use more flexible.

UNIX uses overlays and swapping to replace the unused program. However, it is facing external fragmentation problem and solve by loading the program into memory by using best fit algorithm.

Besides, UNIX also fully utilized the virtual memory (physical memory and swap space) by using demand paging. It allows user to store physical memory in the hard disk because the RAM memory was always insufficient.

Summary

• Classical UNIX scheduling
– user mode: priority-based, time-sharing, preemptive • the process with the highest priority runs first
• round-robin time-sharing scheduling between processes at the same prio. level
• priority is calculated based on previous CPU usage and the nice value
– kernel mode: fixed priority, non-preemptive
• sleep priority assigned to resources will be given to awaking processes
– simple, avoids starvation, handles I/O jobs very well
– no SMP support, does not scale well, no support for spec. app. needs
• Modern UNIX schedulers
– modular
– several scheduling classes according to applications' needs
– supports multi-cpu, multi-core systems (including CPU affinity)
– better resource allocation (guaranteed CPU resources) – schedule threads

THE END

National Education Society (R), JNN College of Engineering, Shivamogga

Jawaharlal Nehru National College of Engineering
Department of Electronics and Communication

Date:18/4/2019

REPORT

The department of Electronics and Communication Engineering of Jawaharlal Nehru National College of Engineering, Shivamogga in association with IETE Shimoga Centre has organized an Industrial trip to Vaarahi power plant, Hosangadi to 4th semester students of ECE on 16/4/2019. The team lead by Dr.P.Manjunatha ,Professor and Head dept of ECE accompanied by four faculty members Mrs. Prema K N, Mrs.Smitha S M, Mrs.Shwetha B and Mr. Sunil M D departed the city at around 7AM on 16/4/2019. Almost 115 students were part of the event.

The team arrived at Vaarahi power plant at 11.00 AM. After completing all the formal procedure to enter the power plant they sent us inside the plant by two groups, each group consists of around 60 members. First we visited the control room in the power plant, there the engineers explained the overall plan of power generation, amount of power generation and power distribution methods through a video presentation.

Mr. Prasanna and one more engineer of Vaarahi power project explained us the details and operation of all the machineries present in the project for the generation of power in detail. The engineers also explained the frequency ranges and power generation depends on the water levels and water flow. The students got good knowledge about the hydraulic power generation and its advantages. The team left the power plant at 5.30 PM. All students were fascinated and overwhelmed by the visit.

(Dr. P. Manjunatha)

HOD,Dept. of ECE

Chairman, IETE Shimoga Centre

Head of the Department
Electronics and Communication
J.N.N. College of Engineering
SHIMOGA-577 204.

KPCL
ಕರ್ನಾಟಕ ವಿದ್ಯುತ್ ನಿಗಮ ನಿಯಮಿತ
KARNATAKA POWER CORPORATION LTD.,
(A premier power generating company of Government of Karnataka)
CIN U85110KA1970SGC001919

ದಿನಾಂಕ: 09.04.2019

ಸಂಖ್ಯೆ:ಎ1 ಎ6 ಎ ಸಿಸಿ:18 / 140

ಪ್ರಾಂಶುಪಾಲರು,
ಜೆ.ಎನ್.ಎನ್. ಕಾಲೇಜ್ ಆಫ್ ಇಂಜಿನಿಯರಿಂಗ್,
ನವುಲೆ,
ಶಿವಮೊಗ್ಗ – 577 204
ದೂರವಾಣಿ: 08182-276707 ಫ್ಯಾಕ್ಸ್: 08182-222450
ಮೊಬೈಲ್: 8277324422/7022620220

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

ಮಾನ್ಯರೆ,

ವಿಷಯ: ವಾರಾಹಿ ಯೋಜನಾ ಪ್ರದೇಶವನ್ನು ಸಂದರ್ಶಿಸಲು ಅನುಮತಿ – ಕುರಿತು.
ಉಲ್ಲೇಖ: ನಿಮ್ಮ ಪತ್ರ ಸಂಖ್ಯೆ:JNNCE/ECE/34/2019-20 ದಿನಾಂಕ: 04.04.2019.

*****

ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು ಸಂದರ್ಶಿಸಲು ತಾವು ಬರೆದುಕೊಂಡ ಉಲ್ಲೇಖ ಪತ್ರದಲ್ಲಿ ತಿಳಿಸಿರುವಂತೆ **ಮಾನಿಡ್ಯಾಂ ಪವರ್ ಹೌಸ್/ಮಾಸ್ತಿಕಟ್ಟೆ ಮತ್ತು ವರಾಹಿ ಭೂಗರ್ಭ ಜಲ ವಿದ್ಯುದಾಗಾರ/ಹೊಸಂಗಡಿ** ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು **ದಿನಾಂಕ:16.04.2019**ರಂದು ತಮ್ಮ ಸಂಸ್ಥೆಯ 2ನೇ ವರ್ಷದ ಎಲೆಕ್ಟ್ರಾನಿಕ್ಸ್ & ಕಮ್ಯೂನಿಕೇಷನ್ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗದ **152** ವಿದ್ಯಾರ್ಥಿಗಳು ಹಾಗೂ **10** ಉಪನ್ಯಾಸಕರು/ಸಿಬ್ಬಂದಿ ಸೇರಿ ಒಟ್ಟು **162** ಸದಸ್ಯರಿಗೆ ಎರಡು ತಂಡಗಳಾಗಿ ವೀಕ್ಷಿಸಲು ಈ ಮೂಲಕ ಅನುಮತಿ ನೀಡಲಾಗಿದೆ. [**ಭೇಟಿಯ ಸಮಯ: ಬೆಳಿಗ್ಗೆ 9.00 ಘಂಟೆಯಿಂದ 12.00 ಘಂಟೆಯವರೆಗೆ ಮತ್ತು ಮಧ್ಯಾಹ್ನ 2.00 ಘಂಟೆಯಿಂದ 4.30 ಘಂಟೆಯವರೆಗೆ ಮಾತ್ರ – ಶನಿವಾರ ಬೆಳಿಗ್ಗೆ ಮಾತ್ರ**].

ಈ ಅನುಮತಿಯು ಕೆಳಗಿನ ನಿಬಂಧನೆಗಳಿಗೆ ಒಳಪಟ್ಟಿರುತ್ತದೆ.

1] ಸಂಸ್ಥೆಯ ಮುಖ್ಯಸ್ಥರಿಂದ ಪಡೆದಿರುವ ಗುರುತಿನ ಚೀಟಿಯನ್ನು (**Identity card**) ಹಾಜರು ಪಡಿಸಲು ಸೂಚಿಸಲಾಗಿದೆ. ಗುರುತಿನ ಚೀಟಿ ಇಲ್ಲದಿದ್ದ ಪಕ್ಷದಲ್ಲಿ ಮುಖ್ಯಸ್ಥರಿಂದ ದೃಢೀಕರಿಸಿರುವ ವಿದ್ಯಾರ್ಥಿಗಳ ಮತ್ತು ಉಪನ್ಯಾಸಕರ ಹೆಸರುಗಳ ಪಟ್ಟಿಯನ್ನು ಕಡ್ಡಾಯವಾಗಿ ಹಾಜರು ಪಡಿಸಲು ಸೂಚಿಸಲಾಗಿದೆ.

2] ಪಟ್ಟಿಯಲ್ಲಿರುವವರನ್ನು ಭಾರತೀಯ ಪೌರರೆಂದು ಧೃಢೀಕರಿಸಬೇಕು. ಇಲ್ಲದ ಪಕ್ಷದಲ್ಲಿ ಅನುಮತಿಯನ್ನು ನಿರಾಕರಿಸಲಾಗುವುದು. ವಿದೇಶಿಯರಿಗೆ ಯೋಜನಾ ಪ್ರದೇಶಗಳಿಗೆ ಅನುಮತಿ ನೀಡಲಾಗುವುದಿಲ್ಲ.

3] ವಿಡಿಯೋ/ಮೊಬೈಲ್/ಕ್ಯಾಮರಗಳನ್ನು ಯೋಜನಾ ಪ್ರದೇಶದ ಒಳಗೆ ತೆಗೆದುಕೊಂಡು ಹೋಗುವುದನ್ನು ಹಾಗೂ ಛಾಯಾಚಿತ್ರಗಳನ್ನು, ಸೆಲ್ಫಿ ತೆಗೆಯುವುದನ್ನು ನಿಷೇಧಿಸಲಾಗಿದೆ.

4] ವಿದ್ಯಾರ್ಥಿಗಳು **16ವರ್ಷ** ಮೇಲ್ಪಟ್ಟವರಾಗಿದ್ದು ಸಂಸ್ಥೆ/ಕಾಲೇಜು ಮುಖ್ಯಸ್ಥರುಗಳು ಕಡ್ಡಾಯವಾಗಿ ತಂಡದೊಂದಿಗೆ ಇರಬೇಕು. ವಿದ್ಯಾರ್ಥಿಗಳ ರಕ್ಷಣೆಯ ಜವಾಬ್ದಾರಿ ಸಂಸ್ಥೆ/ಕಾಲೇಜಿನ ಮುಖ್ಯಸ್ಥರುಗಳಿಗೆ ಸೇರಿರುತ್ತದೆ.

5] ಯೋಜನಾ ಪ್ರದೇಶದಲ್ಲಿ ಆಹಾರ ಸ್ವೀಕರಿಸುವುದು, ಮನೋರಂಜನೆ ಮತ್ತು ಖಾಸಗಿ ವಾಹನಗಳಿಗೆ ಅವಕಾಶವಿರುವುದಿಲ್ಲ.

6] ಯೋಜನಾ ಪ್ರದೇಶದಲ್ಲಿ ನಿಗಮದ ಯಾವುದೇ ಆಸ್ತಿ–ಪಾಸ್ತಿಗೆ ಹಾನಿ ಉಂಟುಮಾಡುವಂತಿಲ್ಲ. ಒಂದು ವೇಳೆ ಪ್ರಾಣ ಹಾನಿ ಮತ್ತು ಯಾವುದೇ ಅಹಿತಕರ ಘಟನೆಗಳು ಸಂಭವಿಸಿದಲ್ಲಿ ಈ ಘಟನೆಗಳಿಗೆ ಸಂಸ್ಥೆಯ/ಕಾಲೇಜಿನ ಮುಖ್ಯಸ್ಥರು ಸಂಪೂರ್ಣ ಜವಾಬ್ದಾರರಾಗಿರುತ್ತೇವೆಂದು ಹಾಗೂ ನಿಗಮದ ಆಸ್ತಿ–ಪಾಸ್ತಿಗೆ ಧಕ್ಕೆ ಉಂಟು ಮಾಡಿದಲ್ಲಿ ಸಂಪೂರ್ಣ ವೆಚ್ಚವನ್ನು ಭರಿಸಿ ಕೊಡಲಾಗುವುದೆಂದು ಪ್ರಮಾಣ ಪತ್ರದ ಮುಚ್ಚಳಿಕೆಯನ್ನು ಭೇಟಿ ನೀಡುವ ಸಂದರ್ಭದಲ್ಲಿ ಯೋಜನಾ ಪ್ರದೇಶದ ಮುಖ್ಯಸ್ಥರುಗಳಿಗೆ ಕಡ್ಡಾಯವಾಗಿ ನೀಡತಕ್ಕದ್ದು. ನಿಗಮ ಯಾವುದೇ ರೀತಿಯಲ್ಲಿ ಜವಾಬ್ದಾರಿಯನ್ನು ಹೊಂದಿರುವುದಿಲ್ಲ.

ತಾವುಗಳು ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು ಪ್ರವೇಶಿಸಿದ ನಂತರ ಭೇಟಿಯ ವ್ಯವಸ್ಥೆಗಾಗಿ ಕಾರ್ಯನಿರ್ವಾಹಕ ನಿರ್ದೇಶಕರು (ಪೈಡಲ್)ವರಾಹಿ, ಕೆಪಿಸಿಎಲ್, ಹೊಸಂಗಡಿ–576 282, ಉಡುಪಿ ಜಿಲ್ಲೆ ದೂರವಾಣಿ ಸಂಖ್ಯೆ: 08259-288242 ಇವರನ್ನು ಸಂಪರ್ಕಿಸುವುದು.

ವಂದನೆಗಳೊಂದಿಗೆ,

ತಮ್ಮ ವಿಶ್ವಾಸಿ,
ಕರ್ನಾಟಕ ವಿದ್ಯುತ್ ನಿಗಮ ನಿಯಮಿತದ ಪರವಾಗಿ,

ಉಪ ಪ್ರಧಾನ ಪ್ರಬಂಧಕರು (ಕಾರ್ಪೊರೇಟ್ ಕಮ್ಯುನಿಕೇಷನ್ಸ್)

'ಶಕ್ತಿ ಭವನ', ನಂ. 82, ರೇಸ್ ಕೋರ್ಸ್ ರಸ್ತೆ, ಬೆಂಗಳೂರು–560 001. ದೂರವಾಣಿ : 080-2225 6568 ಫ್ಯಾಕ್ಸ್ : 080-2225 2144
'Shakthi Bhavan', # 82, Race Course Road, Bengaluru-560 001. Tel. : 080-2225 6568 Fax : 080-2225 2144
E-mail : kpcicccmpa@gmail.com Website : www.karnatakapower.com

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ
NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.
Jawaharlal Nehru National College of Engineering, Shivamogga
(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)
ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.
(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref No.: JNNCE/ECE/34/2019-20 Date: 04-04-2019

To,

The General Manger
Corporate communications
Karnataka Power Corporation Ltd.,
Shakthi Bhavan
#82, Race course Road
Bangalore 577435
Ph: 080-22256568, Fax: 080-222521444

Dept. of Electronics & Communication Engineering JNNCE SHIVAMOGGA-577 204

Respected Sir,

Subject: Requisition for revised permission date to visit Vaarahi Power Plant and Mani Dam .

Ref : your letter No:A1 A6 A CC:528/05 dated :1.4.2019

With respect to the above subject, we received your permission letter **No:A1 A6 A CC:528/05 dated :1.4.2019** on 4th April due to postal delay, which had the date of visit is also same.So kindly permit us to visit Vaarahi Power plant on 16th April 2019. About 152 2nd year BE students of our branch intend to visit the esteemed Vaarahi Power plant on 16th April 2019 along with staff members. This visit will give them a direct practical exposure of power plant which is installed underground. They also intend to visit Mani Dam on the same day.

Please grant the permission to visit the power plant and Mani Dam.

Thanking you

Yours faithfully,

4-4-19
Dr. Manjunatha P
Head of the Department
ECE JNNCE, Shimoga

Dr. Manjunatha. P
B.E., M.E., Ph.D. (IIT Bombay)
Prof. & Head, Department of E&CE
J.N.N. College of Engineering
SHIVAMOGGA.

Dr.H R Mahadevaswamy
Principal,
Jawaharlal Nehru National College of Engineering, Shivamogga.

Encl: List of Visitors

Contact Persons: Prema K N: Mob:8277324422
Email:premakn@jnnce.ac.in
Smitha S M:Mob:7022620220
smithasm@jnnce.ac.in

ನವುಲೆ, ಶಿವಮೊಗ್ಗ – 577 204, ಕರ್ನಾಟಕ
Navule, Shivamogga - 577 204, Karnataka
E - mail : Principal@jnnce.ac.in Website : www.jnnce.ac.in
☎ : 08182 - 276707 / 08 / 09 Fax : 08182 - 222450

List of Students and staff members visiting Varahi Power House and Mani Dam on

Sl.No	USN	Name
1	4JN16EC035	KARTHIK M T
2	4JN16EC045	MANJUNATHA VIJAYAPPA BANGERA
3	4JN16EC087	SHRIDHARA S
4	4JN16EC102	TANIYA SHAIKH
5	4JN16EC440	SRILEKHA H C
6	4JN17EC001	AALIYA TAZEEN
7	4JN17EC002	AISHWARYA CHAVAN K M
8	4JN17EC003	AISHWARYA JODANGI
9	4JN17EC004	AJAY S R
10	4JN17EC005	AKASH K
11	4JN17EC006	AKSHATHA R
12	4JN17EC007	AKSHAY VENKATRAMANA BHAT
13	4JN17EC008	AMULYA U
14	4JN17EC009	ANILGOUDA AGASIMUNDIN
15	4JN17EC010	ANURAG PANDEY
16	4JN17EC011	ANUSHA H M
17	4JN17EC012	APEKSHA C S
18	4JN17EC013	ARPANA A P
19	4JN17EC014	ARPITHA M P
20	4JN17EC015	ASHUTOSH KUMAR
21	4JN17EC016	BHUMIKA S B
22	4JN17EC017	BRUNDA N C
23	4JN17EC018	CHANDAN P
24	4JN17EC019	CHANDANA GOWDA N
25	4JN17EC020	DARSHAN B R
26	4JN17EC021	DEEPA B
27	4JN17EC022	DHRAVYA B S
28	4JN17EC023	DRUSTI G J
29	4JN17EC024	DUGGESH M P
30	4JN17EC025	GURUPRASAD R
31	4JN17EC026	HARSHA M B
32	4JN17EC027	K S ANOOP
33	4JN17EC028	KARTHIK BHARADWAJ A R

Sl.No	USN	Name
34	4JN17EC029	KARTHIK O
35	4JN17EC030	KAVYA M
36	4JN17EC031	KAVYASHREE M
37	4JN17EC032	KEERTHANA S
38	4JN17EC033	KIRAN KUMAR K S
39	4JN17EC034	KOMALA PATEL S
40	4JN17EC035	LAKSHMI H S
41	4JN17EC036	LAVANYA T
42	4JN17EC037	LIKITHA M
43	4JN17EC038	MANISHA K H
44	4JN17EC039	MANOJ M
45	4JN17EC040	MASOUDA NOUSHIN
46	4JN17EC041	MEDINI YADIYAL
47	4JN17EC042	MEGHA G N
48	4JN17EC043	MEGHANA B M
49	4JN17EC044	MOHAMMED JUNAID
50	4JN17EC045	MOHAMMED SAFEER ABBAS
51	4JN17EC046	MOHAMMED ZEESHAN
52	4JN17EC047	MOHAN KUMAR H P
53	4JN17EC048	MONIKA K P
54	4JN17EC049	NAGANDHIKA U
55	4JN17EC050	NIKHITHA V MELIGE
56	4JN17EC051	NIMRA KULSUM
57	4JN17EC052	NISARGA T M
58	4JN17EC053	PAVAN E V
59	4JN17EC054	PAVANA KUMARA
60	4JN17EC055	PAVANKUMAR B J
61	4JN17EC056	POOJA H K
62	4JN17EC057	PRAJWAL A C
63	4JN17EC058	PRAJWAL A SHETTY
64	4JN17EC059	PRAJWAL H S
65	4JN17EC060	PRAJWAL S YALLUR
66	4JN17EC061	PRAJWAL T PPATANAKAR
67	4JN17EC062	PRATHIMA P
68	4JN17EC063	PRATHISHTA M

Sl.No	USN	Name	Sl.No	USN	Name
69	4JN17EC064	PRIYANKA SURESH KORI	113	4JN17EC112	VINAY KUMAR KOULUR
70	4JN17EC065	RACHANA KR	114	4JN17EC113	VINAY N M
71	4JN17EC066	RACHANA R	115	4JN17EC114	VINUTHA D H
72	4JN17EC067	RAKSHITA SURESH DODDAMANI	116	4JN17EC115	VISMAYA M PRIYA
73	4JN17EC068	RAKSHITH N	117	4JN17EC116	YASHAWANTH G S
74	4JN17EC069	RAMAMANOJ Y S	118	4JN17EC117	MISBAH AASHIQ
75	4JN17EC070	RAMYA K	119	4JN17EC118	NADEEM SHAFI DAR
76	4JN17EC071	RAMYASHREE K U	120	4JN17ME064	PAVAN GANESH KULKARNI
77	4JN17EC072	RANJANA J	121	4JN17ME101	SUJAN G BHARGAV
78	4JN17EC073	RASHMI R	122	4JN17EE030	PUNITH K N
79	4JN17EC074	RESHMA R (Ravi K)	123	4JN17EE044	SHUBHAM SHARMA
80	4JN17EC075	ROOPASHREE	124	4JN17IS005	AKASHADEEPA N
81	4JN17EC076	RUKHIYA KHANUM	125	4JN17IS038	MANOJ KUMAR R
82	4JN17EC078	SAGAR K	126	4JN18EC400	ANUP V N
83	4JN17EC079	SAI RAJ S V	127	4JN18EC401	ARSHIYA NAAZ
84	4JN17EC080	SALEEMULLA K G	128	4JN18EC402	BHARATH B N
85	4JN17EC081	SANCHITHA G R	129	4JN18EC403	BHOOMIKA S N
86	4JN17EC083	SANDHYASHREE M C	130	4JN18EC404	GANESH J M
87	4JN17EC084	SANJANA EDIG M	131	4JN18EC405	KIRANA S
88	4JN17EC085	SANJANA M	132	4JN18EC406	LOKESHA S
89	4JN17EC086	SANJAY D GOWDA	133	4JN18EC407	MOHAMMED ARBAZ BASHA
90	4JN17EC087	SHABARISH REDDY B S	134	4JN18EC408	MOHAN RAJ M
91	4JN17EC088	SHREE HARI H M	135	4JN18EC409	MONIKA L N
92	4JN17EC089	SHREYA H S	136	4JN18EC410	MUDDUSHRI M
93	4JN17EC090	SHRIKANTH VAIDYA S M	137	4JN18EC411	NAVYASHRI S R
94	4JN17EC092	SHRUTHI B	138	4JN18EC412	NIKHIL MARIAN D
95	4JN17EC093	SHRUTI SUBRAHMANYA REDDI	139	4JN18EC413	NIKITHA D
96	4JN17EC094	SIDDESH N P	140	4JN18EC414	PRASHANTHA R
97	4JN17EC096	SNEHA N	141	4JN18EC415	RAGHU B
98	4JN17EC097	SNEHA T P	142	4JN18EC416	RAKSHITH K
99	4JN17EC098	SOUPARNIKA I C	143	4JN18EC417	RATHAN KUMAR H R
100	4JN17EC099	SUBHASH M B	144	4JN18EC418	SACHINKUMAR H P
101	4JN17EC100	SUBRAMANYA C	145	4JN18EC420	SHAMBHU NADAGER
102	4JN17EC101	SUCHITRA SRINIVAS	146	4JN18EC423	SINDHU D T
103	4JN17EC102	SUHAS S	147	4JN18EC426	SUNIL KUMARA D T
104	4JN17EC103	SUJEETH U S	148	4JN18EC419	SANJANAGOWDA R
105	4JN17EC104	SWATHI S	149	4JN18EC421	SHRIYASHA
106	4JN17EC105	TEJASWINI D O	150	4JN18EC422	SINCHANA K A
107	4JN17EC106	THEJASWINI A D	151	4JN18EC424	SMITHA M M
108	4JN17EC107	U KAVYA	152	4JN18EC425	SUDEEP S
109	4JN17EC108	USHA			
110	4JN17EC109	USHA NUCHIN			
111	4JN17EC110	VARSHITHA R			
112	4JN17EC111	VIGNESH B			

Staff members List:

1. Dr.P Manjunatha
2. Sunil M D
3. Roopa B S
4. Smitha S M
5. Prema K N
6. S B Nalina
7. Swetha B
8. Shwetha H R
9. Sathish Kumar H G
10. Nanjundappa

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

HOD

4-4-19

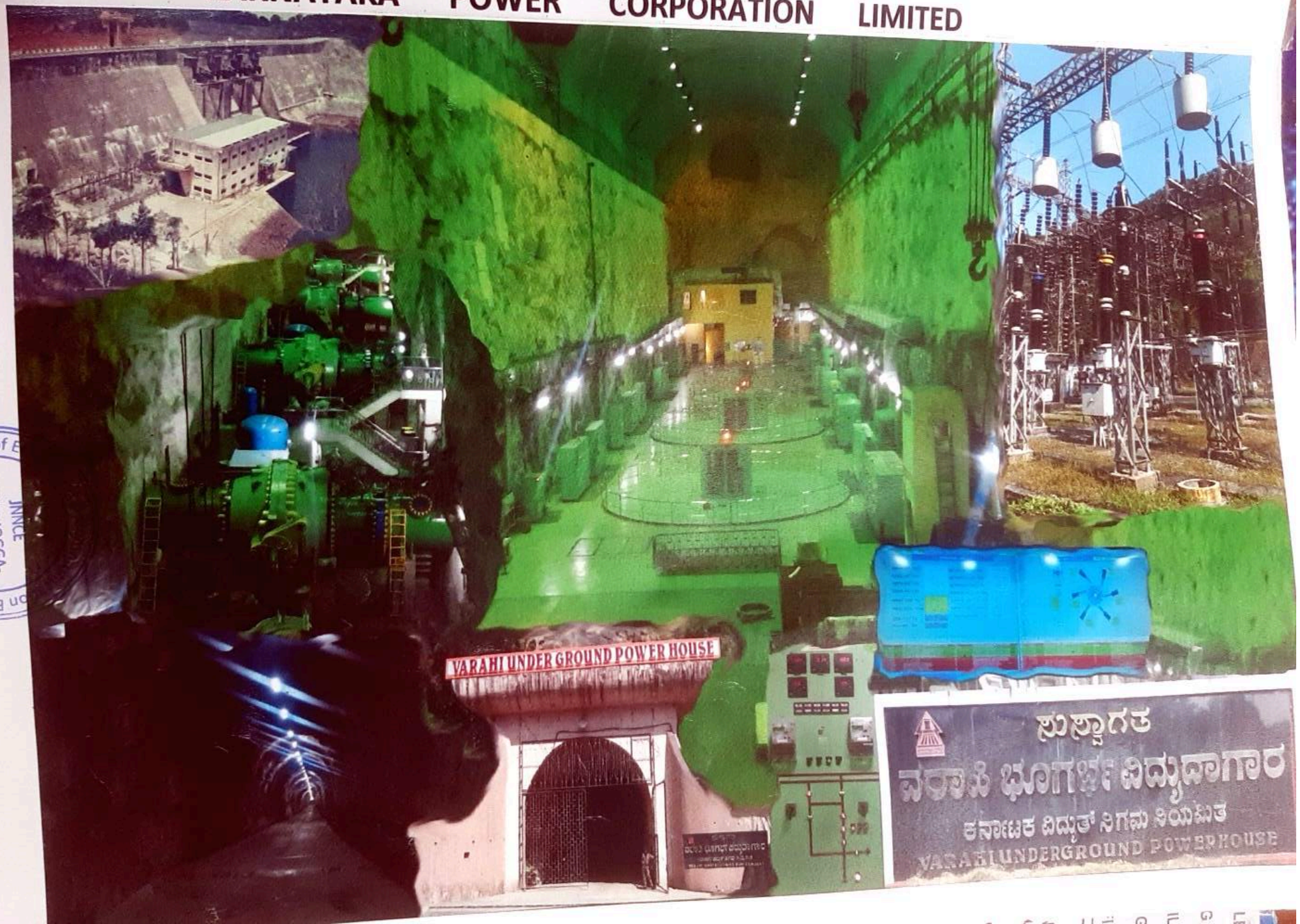
Department of ECE, JNNCE

Principal, JNNCE

Principal
Jawaharlal Nehru National C
of Engineering, Shivamo

Dr. Manjunatha. P.
B.E., M.E., Ph.D. (IIT Bombay)
Prof. & Head, Department of E&CE
J.N.N. College of Engineering
SHIVAMOGGA.

KARNATAKA POWER CORPORATION LIMITED



JNN College of Engineering

Department of Electronics and Communication

Industrial Trip to MCF Hassan on 29/03/19 for 6th Semester students

Total Expenses of Industrial trip

Si No	Expenditure	Amount
1	Food expenses+fried rice parcel	9395-00
2	Miscellaneous(Cocunut+lemon+focus light+biscuits)	140-00
3	Bus Fare	20000-00
4	Driver (Byata +Expenses)	2115-00
5	Oranges	721-00
6	Paper plates +bin covers	255-00
7	Parking	280-00
8	Total	32906-00

Total number of students 69

Amount collected 69*500/- =34500-00

(-) Total expenses=32906-00

Remaining amount= 1594-00

KARNATAKA POWER CORPORATION LIMITED

Sharavathy Valley Project

Annexure 'A'

Visitors to protected Establishment

VISITOR ID: 17201

Visitors Signature

3 PERMITTED TO SEE :

4 DATE AND PERIOD OF VISIT :
06-OCT-18 TO 06-OCT-18

5 TIME OF VISIT :
10:40 TO 17:30

6 REASON OF VISIT :

7 CLEARANCE CONFIRMED :

8 VISIT APPROVED :

9 VEHICAL NO :

SECURITY OFFICER
K.P.C.L JOGFALLS-577435

Signature

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

INSTRUCTIONS TO VISITORS

1. Photography is strictly prohibited in the project area.

2. Corporation will not be responsible for any of the damages/losses accidents etc., caused either to the visitors or to their vehicles properties etc., in the project area.

3. Passes will be issued to the visitors between 9-00 AM to 12-00 Noon and 2-30 PM to 5-00 PM.

4. Visitors are requested to be physically present while issuing passes if demanded with their vehicles for scrutiny.

5. Vehicles owners or drivers should show the documents of the vehicles if demanded by the pass issuing authority.

6. Discretion of the pass issuing authority will be final for permitting to enter the project area.

Date: 06/10/2018

Jawaharlal Nehru National College of Engineering
Shivamogga.

Department of Electronics & Communication Engineering

Report of "One day Industrial visit to Sharavathi Power Generation unit (SGS)"

The department of ECE had organized a one day Industrial Visit to Sharavathi Power Generation Unit" for the Fifth Semester students of ECE Dept, JNNCE, Shimoga on 06/10/2018 at ECE department. In total 52 students have actively participated in this Industrial visit.

The Industrial visit was initaited by Dr. P. Manjunatha, HOD of ECE Department, Prashanth G S, Asst. Prof, Dept of ECE , Mrs Roopa B S,Asst. Prof, Dept of ECE and Mrs. Prema K N, Asst. Prof, Dept of ECE, and were also present in the function.

For industrial visit, we left shimoga at 7.30AM by bus and reached Jog by 10.30 AM. Finished all the formalities in the office of sharavathi power station. The PASS to enter the sharavathi power generation unit was given. From the office, the sharavathi power generation unit is around 8 km. Reached the sharavathi power station unit by 11.30 AM. **Mr.Ramesh H M**, Assist Engineer, (Electrical) office of EE(PS&O), Sharavathi power generation unit, Jog falls, welcomed us and explained the generation of hydroelectric power by flowing water. **Mr.Ramesh H M,** initially explained the requirements of power in Karnataka daily. Sir, explained that totally 10,000 MW of power is required daily in Karnataka, SGS will generate 10% of power required by Karnataka daily, i.e over 1000 MW is generated from SGS daily . SGS is largest hydroelectric power unit in Karnataka. Hydroelectric plant produces electricity from the water pressure on the turbines. It uses water pressure to turn the propellers of a machine called a turbine. As the turbine spins, it turns a metal shaft connected to an electric generator, which is basically a motor that produces electricity. Sharavathi power station has 10 water chambers to which 10 separate turbines are connected to generate power separately. Each water chamber as a special passageway called the penstock, with the help of penstock, the flow of water is controlled. Each Chamber with turbine generates a 100 MW of power. i.e. totally from 10 units 10000 MW of power generated.

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

06-01-18

Photos

Sharvathi Power Station unit

ISRO SATELLITE CENTRE
BANGALORE

Rajendra Hulyal
Group Head
Programme, Planning & Evaluation Group

☎ 080-2508 2126
Fax No. 080 – 2520 5261

20 February 2018

To,
Dr. Manjunatha P
Profesor & Head Department of E&CE ,
Jawaharlal Nehru National College of Engineering,
Shimoga.
Sir / Madam,

SUB: Permission to visit ISRO Satellite Centre – Reg.

Department of Electronics & Communication Engineering JNNCE SHIVAMOGGA-577204

We are in receipt of your post / email letter dated 20.02.2018 requesting permission to visit on the **following date.**

07.03.2018	**14.00hrs to 16.00 Hrs**

Please provide details of team members and faculty members along with an authorization letter from the Instructor to the Leader of the team (co-ordinator) restricted to **100** members only. subject to the following conditions

The team may report to Reception Counter of this Centre 15 minutes in advance in order to complete the administrative formalities for issuing entry passes.

1. **You are requested to strictly adhere to the time schedule mentioned above.**
2. **In case of any exigencies, we may cancel the above visit without any intimation.**
3. **Carrying Camera and taking photography inside this Centre is strictly prohibited.**
4. **Mobile phones and electronic gadgets are not allowed to be taken inside.**
5. **The visitors should declare items to be carried if any and seek permission, while entering this Center to the security personnel for checking.**
6. **No foreign nationals are allowed.**
7. **No Family members will be allowed inside this centre.**
8. **After the visit Acknowledgement letter will not be issued from the organization.**

Please note that our office is located on Old HAL Airport Road, Bangalore-560 017 next to National Aerospace Laboratories (NAL). Our telephones Nos. are 080, 25084469 & 25084470.

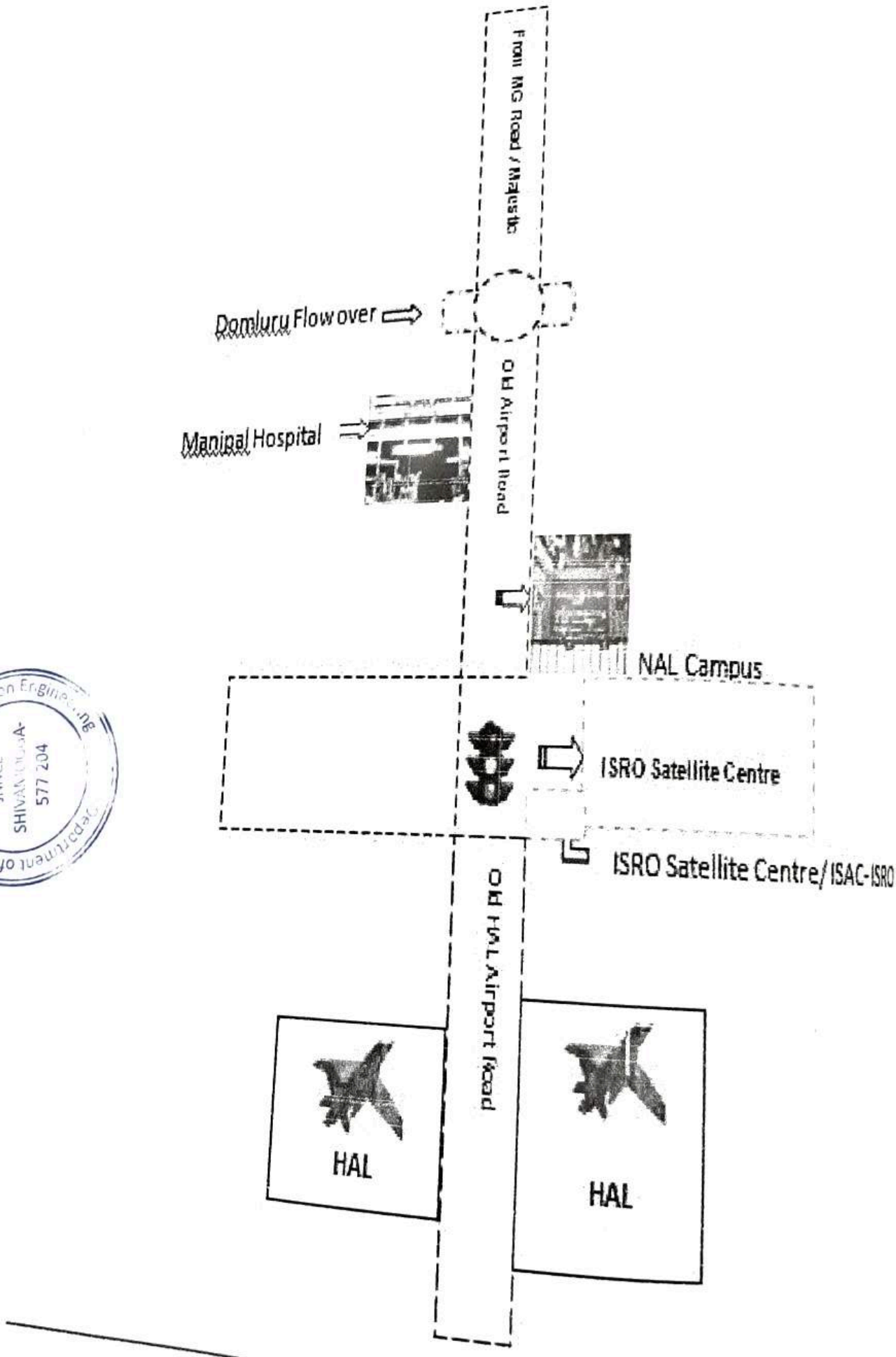
The Professor accompanying the Students may kindly contact the Reception Counter of this Centre to complete the administrative formalities and for issue of Entry pass in time. Kindly acknowledge the receipt of this letter.

Yours faithfully,

Sd/-
(Rajendra Hulyal)

Copy to:
Group Director – SCG / SIG, CGM – Facilities
Administrative Officer (PRO), ISRO Satellite Centre, Bangalore-17.

Note please see route map is attached



ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ
NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.
Jawaharlal Nehru National College of Engineering, Shivamogga
(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)
ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.
(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

To,

ISAC
Bangalore

From,

The Principal,
JNNCE,
Shivamogga

Dept. of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

Subject: Requesting you to provide permission to visit ISAC.

As a part of Industrial visit, our students of B.E (Electronics and Communication Engg..) would like to visit ISAC. This will help our students to know ISAC, facilities, technologies and also enhances their knowledge in that area.

Possible dates for visit are 26/2/2018 or 3/3/2018, please suggest other dates if the slot is not available on the above said dates.

List of Students and Staffs are attached.

Thanking you,

Your's faithfully,

(Dr.H.R.Mahadevaswamy)

ನವುಲೆ, ಶಿವಮೊಗ್ಗ – 577 204, ಕರ್ನಾಟಕ
Navule, Shivamogga - 577 204, Karnataka

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ
NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.
Jawaharlal Nehru National College of Engineering, Shivamogga
(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)
ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.
(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

Faculty members :

1. Sunil M D Assistant professor, E&CE Dept
2. Mallesh Kumar K S, Regional Coordinator.

Student List

Sl no	USN	Student Name	Sl no	USN	Student Name
1	4JN14EC062	POOJA M M	24	4JN15EC031	KARTHIK N
2	4JN14EC078	RENUKA D P	25	4JN15EC032	KAVERI S T
3	4JN15EC001	ADARSH B P	26	4JN15EC033	KAVYA A
4	4JN15EC003	ADITYA K B	27	4JN15EC039	MAMATHA R
5	4JN15EC005	ANANYA K	28	4JN15EC041	MANOJ KUMAR
6	4JN15EC006	ANNAPURNA R HAVANUR	29	4JN15EC046	NANDINI M
7	4JN15EC008	ANUSH A L	30	4JN15EC049	POOJA K P
8	4JN15EC009	ANUSH GOWDA B M	31	4JN15EC050	POOJA PAI
9	4JN15EC011	ASHWITHA M	32	4JN15EC051	POOJA R
10	4JN15EC012	ASIMA SIDDIQ	33	4JN15EC052	POOJA S
11	4JN15EC014	BHAVANA S	34	4JN15EC053	POOJA G T H
12	4JN15EC015	CHAITRA B R	35	4JN15EC054	POORNIMA MG
13	4JN15EC016	CHAITHRA S V	36	4JN15EC056	PRAKASH C
14	4JN15EC017	CHANDANA C	37	4JN15EC106	AKHILESH S (COB)
15	4JN15EC018	DEEKSHA NAYAK	38	4JN16EC400	ANAND HAVALADAR
16	4JN15EC019	DEEKSHITHA S	39	4JN16EC403	CHAITHRA N S
17	4JN15EC020	DEEPTHI C SHETTY	40	4JN16EC404	CHAITRA S
18	4JN15EC021	DEEPTHI DATTA	41	4JN16EC405	DEEPA M C
19	4JN15EC022	DIVYA C SHETTY	42	4JN16EC407	HARSHITHA S
20	4JN15EC025	GAGANA M L	43	4JN16EC413	MEGHANA R
21	4JN15EC029	HARSHITA M K	44	4JN16EC424	PRIYANKA H R
22	4JN15EC030	K R ROHAN	45	4JN16EC425	PRIYANKA N
23	4JN16EC432	SANJAY S	46	4JN15EC094	SYEDA SABIHA K

Department of Electronics & Communication JNNCE SHIVAMOGGA-577 204

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ
NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.
Jawaharlal Nehru National College of Engineering, Shivamogga
(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)
ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.
(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

47	4JN16EC437	SHILPA L	73	4JN15EC095	TEJASWINI B R
48	4JN16EC438	SHOBHITH M	74	4JN15EC096	TEJASWINI BAI P
49	4JN15EC057	PRAKRUTI G K	75	4JN15EC097	UME KULSUM
50	4JN15EC059	PRIYANKA V G	76	4JN15EC099	VIDHYASHREE H B
51	4JN15EC062	RAHUL A POOJAR	77	4JN15EC102	YASHASWINI S R
52	4JN15EC063	RAHUL H A	78	4JN16EC401	BEERAPPA MAJJAGI
53	4JN15EC064	RAJASHRI M	79	4JN16EC406	GAGANA S
54	4JN15EC066	RAJESHA M U	80	4JN16EC409	K A SANGEETHA
55	4JN15EC067	RAKSHITA B	81	4JN16EC410	KARTHIKA M
56	4JN15EC068	RANJITH KUMAR K M	82	4JN16EC411	KAVANA B M
57	4JN15EC069	REHANA BEGUM	83	4JN16EC412	MEGHANA N
58	4JN15EC070	RIDHI S JAIN	84	4JN16EC415	MOHAN N
59	4JN15EC071	RUCHIKA E	85	4JN16EC416	NAGENDRA H S
60	4JN15EC072	SACHIN KUMAR K	86	4JN16EC417	NANDAN H R
61	4JN15EC073	SAHANA H S	87	4JN16EC421	PAVANKUMAR N
62	4JN15EC074	SAHANA N G	88	4JN16EC422	POORNIMA B
63	4JN15EC078	SHREERAKSHA	89	4JN16EC423	PRASHANTH M P
64	4JN15EC080	SHRINIDHI G HEGDE	90	4JN16EC427	RAMYA M
65	4JN15EC081	SINDHU A G	91	4JN16EC428	RAMYA T R
66	4JN15EC082	S SINDHU	92	4JN16EC430	RENUKA M M
67	4JN15EC085	SNEHA S	93	4JN16EC431	SALEEM ISMAIL S
68	4JN15EC086	SRILAKSHMI NAYAKA S R	94	4JN16EC433	SHANKARA C V
69	4JN15EC089	SUPRITH H H	95	4JN16EC436	SHARMILA M BHOUSLE
70	4JN15EC091	SWATHI G S	96	4JN16EC439	SINDHU D V
71	4JN15EC092	SWATHI S Y	97	4JN14EC040	KAVYA H M
72	4JN15EC093	SYEDA AYESHA SAMEERA			

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

JNN College of Engineering

Department of Electronics and Communication

Industrial Trip to MCF Hassan on 29/03/19 for 6th Semester students

Total Expenses of Industrial trip

Si No	Expenditure	Amount
1	Food expenses+fried rice parcel	9395-00
2	Miscellaneous(Cocunut+lemon+focus light+biscuits)	140-00
3	Bus Fare	20000-00
4	Driver (Byata +Expenses)	2115-00
5	Oranges	721-00
6	Paper plates +bin covers	255-00
7	Parking	280-00
8	Total	32906-00

Total number of students 69

Amount collected 69*500/- =34500-00

(-) Total expenses=32906-00

Remaining amount= 1594-00

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

भारत सरकार
अंतरिक्ष विभाग
मुख्य नियंत्रण सुविधा
पो.बो.नं. [illegible]
दूरभाष (08172) 239001 से 04
फैक्स (08172) 239018

इसरो ISRO

Government of India
Department of Space
Master Control Facility
PB #66, Hassan 573 201 India
Telephone (08172) 239001 to 04
Fax (08172) 239018

मु नि सु MCF पत्र अ SAO 39/08

मार्च March 27, 2019

The Principal
Jawaharlal Nehru National College of Engineering,
Navule,
Shivamogga – 577 204

Sir,

विषय **Sub** मुख्य नियंत्रण सुविधा देखने के बारे में Visit to Master Control Facility – reg

सदर्भ **Ref** आपके पत्र /Your Letter दिनांक Dated 22.03.2019

उपरोक्त के सदर्भ में, हमारी सुविधा को देखने के लिए निम्नानुसार अनुमति दी जाती है
With reference to the above, permission is given for visiting our facility as follows

दिनांक **Date**	-	**29.03.2019**
समय **Time**	-	**02:30 hrs**
व्यक्तियों की संख्या **No. of Persons**	-	**82+06 Members**

Department of Electronics & Communication
JNNCE
SHIVAMOGGA
577 204

कृपया नोट करें Please Note That:

1 आपको अनुबद्ध समय के भीतर आना होगा।
You will have to come within the time stipulated.

2 एमसीएफ के भीतर आपकी गतिविधियों के संबध में सुरक्षा के अनुदेशों का सख्त पालन करना होगा।
You will have to strictly follow the instructions of the Security regarding your movement inside MCF

3 आपको अपने आने-जाने के लिए स्वय परिवहन की व्यवस्था करनी होगी।
You will have to make your own arrangements for to and fro transport.

4. हमारी सुविधा हासन नगर से 9 कि.मी. की दूरी पर है एवं अदर या आस–पास किसी भी प्रकार के अल्पाहार की व्यवस्था नही है।
Our facility is 9 kms away from Hassan town and around or inside our facility there is no possibility of getting any refreshments.

5. किसी भी विदेशी को अदर जाने की अनुमति नहीं है।
No foreign Nationals are allowed inside.

6. उपरोक्त उल्लेखित व्यक्तियो को ही अनुमति दी जाएगी।
No. of persons mentioned above only will be permitted.

भवदीय Yours faithfully,

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

(वी दिनेश V Dinesh)
वरि. प्रशा. अधिकारी Sr. Admn. Officer

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ
NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.
Jawaharlal Nehru National College of Engineering, Shivamogga
(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)
ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.
(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

Date:22/03/19

To,

The Director,

Master Control Facility,

Hassan

Department of Electronics & Communication Engg. JNNCE SHIVAMOGGA-577 204

Respected Sir,

Subject: Request to permit industrial visit to MCF, Hassan- Regarding

On behalf of JNNCE, Shimoga, We are writing this letter to your kind concern for getting permission to have an industrial visit to your organization MCF/ISRO. We are here by planning to organize an industrial trip to Master Control Facility, Hassan for 6th sem ECE students JNNCE as a part of academics to excel their knowledge. Our main motive behind this visit is getting actual knowledge of Space Science and Satellite Technology and its Application in communication filed. It is our firm belief that your organization can certainly provide us such information, which will help us and our students to understand satellite communication system and the working and control of the satellites at MCF. We are looking forward for an opportunity, which will help us to get the practical knowledge as well as theoretical approaches.

In this context,we kindly request you to give the permission for visiting MCF on 27thMarch 2019.Nearly 82 students will be the part of the trip accompanied by 6 faculty members. The list of students and faculty members are attached for your reference. Kindly do the needful and oblige.

Thanking you,

Thanking and Regards

Dr. H.R. Mahadevaswamy

Principal

Jawaharlal Nehru National College of Engineering, Shivamogga.

ntact Phone:9886537121, 8147292764

ail id:ujwalaravi2004@jnnce.ac.in
inasb@jnnce.ac.in

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ

NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.

Jawaharlal Nehru National College of Engineering, Shivamogga

(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)

ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.

(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

Student list

Si.No	USN	Name	Si.No	USN	Name
1	4JN16EC056	PAVITHRA D B	44	4JN17EC413	SANGEETHA R
2	4JN16EC061	PRAJNA R	45	4JN17EC412	SACHIN B
3	4JN16EC062	PRAJWAL M	46	4JN16EC026	GOUTHAM S TANTRI
4	4JN16EC063	PRIYANKA N	47	4JN16EC006	ANANTRAYA PRABHAKAR BALGI
5	4JN16EC064	PRIYANKA R J	48	4JN16EC033	HRUTHIK K B
6	4JN16EC065	RACHANA B	49	4JN16EC027	Gururaj A M
7	4JN16EC066	RACHANA S GARA	50	4JN16EC054	NAMRATHA L R
8	4JN16EC067	RAJATH G T	51	4JN16EC017	CHITRA K B
9	4JN16EC068	RANJITHA S	52	4JN16EC052	MURALI S
10	4JN16EC069	RASHMI C V	53	4JN16EC034	KARAN R
11	4JN16EC070	SACHIN R	54	4JN16EC044	MANJUNATHA M J
12	4JN16EC073	SAHANA R	55	4JN16EC019	DEEKSHA A
13	4JN16EC072	SAHANA C R	56	4JN16EC015	CHENNA KALYANA KEERTHI VARDHAN
14	4JN16EC074	SAMPRITHA V SATHISH	57	4JN16EC018	DARSHAN PATIL D
15	4JN16EC077	SANJAY B J	58	4JN16EC022	GAGAN G L
16	4JN16EC078	SANNIDHI M S	59	4JN16EC009	ASHA H N
17	4JN16EC116	VIMA K M	60	4JN16EC038	KUSUMA S
18	4JN16EC083	SHEETHAL H	61	4JN17EC401	ARCHANA V
19	4JN16EC085	SHREYAS B	62	4JN17EC415	SEVANTHI B A
20	4JN16EC086	SHREYAS J S	63	4JN17EC405	DARSHAN R
21	4JN16EC088	SHRISHA T M	64	4JN16EC020	DEEKSHA B GOUDAR
22	4JN16EC089	SHRUTHI G	65	4JN17EC417	SHRAVANI S
23	4JN16EC090	SHUBHAN H K	66	4JN17EC402	B POOJA
24	4JN16EC091	SNEHA P VERNEKAR	67	4JN17EC411	NEHA S
25	4JN16EC092	SONALI S	68	4JN16EC402	Chaitra c
26	4JN16EC093	SOUJANYA M N	69	4JN16EC408	Jahnavi s
27	4JN16EC094	SOWJANYA JAIN	70	4JN16EC046	MEENAKSHI N
28	4JN16EC095	SPANDANA S D	71	4JN16EC025	GOUSEPASHA
29	4JN16EC097	SUHAS S	72	4JN16EC007	ANITHA K P
30	4JN16EC098	SUHAS S NAIR	73	4JN16EC036	KARTHIKA J
31	4JN16EC099	SUPRIYA G A	74	4JN16EC040	MAHANTESH M
32	4JN16EC100	SUSHMITHA S	75	4JN14EC031	Harish G
33	[illegible]	DIVYA N C	76	4JN16EC043	MANJU KARABASAPPA UKKUND

ರಾಷ್ಟ್ರೀಯ ಶಿಕ್ಷಣ ಸಮಿತಿ(ರಿ.), ಶಿವಮೊಗ್ಗ

NATIONAL EDUCATION SOCIETY(R.),SHIVAMOGGA.

Jawaharlal Nehru National College of Engineering, Shivamogga

(Aproved by A.I.C.T.E., and Affiliated to Visvesvaraya Technological University)

ಜವಾಹರ್‌ಲಾಲ್ ನೆಹರು ರಾಷ್ಟ್ರೀಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ, ಶಿವಮೊಗ್ಗ.

(ಎ.ಐ.ಸಿ.ಟಿ.ಇ. ಯಿಂದ ಅನುಮೋದನೆ ಪಡೆದಿದೆ ಮತ್ತು ವಿಶ್ವೇಶ್ವರಾಯ ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯದ ಮಾನ್ಯತೆ ಪಡೆದಿದೆ)

Ref. No.: JNNCE/

34	4JN16EC103	TEJAS KUMAR G N	77	4JN15EC055	Pradyumna H R
35	4JN16EC104	TEKOOR SAPNA R K	78	4JN16EC029	Hanumantha
36	4JN16EC105	THEJASHREE L	79	4JN17EC422	Vijay Kumar G.N
37	4JN16EC106	TILAK PRASAD K M	80	4JN17EC424	Ravish L.S
38	4JN16EC107	ULLAS S	81	4JN16EC113	VARSHITHA C
39	4JN16EC108	USHA H J	82	4JN16EC115	VASUKI H A
40	4JN16EC109	V SHRUTI			
41	4JN16EC110	VAIBHAV JAIN			

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

List of faculty

Sl No	Name	Designation	Department
1	Dr. Manjuatha P	Professor and Head	Electronics & Communication
2	Ujwala B.S	Assistant Professor	Electronics & Communication
3	Nalina S.B	Assistant Professor	Electronics & Communication
4	Anil Kumar J	Assistant Professor	Electronics & Communication
5	Prashanth G.S	Assistant Professor	Electronics & Communication
6	Shwetha B	Assistant Professor	Electronics & Communication

Principal
Jawaharlal Nehru National
College of Engineering, Shivamogga.

National Education Society(R) Jawaharlal Nehru National College of Engineering, Shimoga Date:29/3/2019

Internal Quality Assurance Cell(IQAC)

Department of Electronics and Communication Engineering

Institution of Electronics and Telecommunication Engineers, Shivamogga Centre

Industrial Trip to MCF ,Hassan

Department of Electronics & Communication Engineering JNNCE SHIVAMOGGA 577 204

Student

Sl.No.	USN	Name	Signature
01	4JN16EC026	GAUTHAM STANTRI	Gautham Stantri
02	4JN16EC033	HRUTHIK B	Hruthik
03	4JN16EC052	MURALI.S	Murali.S
04	4JN17EC405	Darshan.R	Darshan
05	4JN16EC034	KARAN.R	Karan
06	4JN16EC025	Mouse pasha	Mouse
07	4JN16EC018	DARSHAN PATIL.D	D.P.D
08	4JN16EC043	Manju.K Ukkund	Manju
09	4JN17EC424	RAVEESHA.L.S	Raveesha.L.S
10	4JN16EC022	GAGAN.G.L	Gagan.GL
11	4JN16EC040	Mahantesh.M.	Mahantesh
12	4JN16EC006	Anantraya.P.Balgi	A.P.Balgi
13	4JN16EC015	CH.KK.Vardhan	Ch.K.K.Vardhan
14.	4JN16EC044	Manjunath.MJ	Manjunatha.M.J
15	4JN16EC027	Gururaj.A.M	Gururaj.A.M.
16	4JN15EC055	PRADYUMNA.HR	Pradyumna
17	4JN16EC029	HAMumanthgowda	Mahesh
18	4JN17EC422	VIJAYKUMAR.G.N	Vijay
19	4JN16EC036	Karthik.J	KarthikJ
20.	4JN14EC031	Harish.G.	Harish
21	4JN17EC417	Shravani.S	Shravani
22	4JN17EC411	Neha.S	Neha
23	4JN16EC054	NAMRATHA.L.R	Namratha.L.R
24.	4JN16EC017	Chitra.K.B	Chitra.K.B.

Jawaharlal Nehru National College of Engineering, Shimoga

Internal Quality Assurance Cell(IQAC)

Date:29/3/2019

Department of Electronics and Communication Engineering

Institution of Electronics and Telecommunication Engineers, Shivamogga Centre

Industrial Trip to MCF ,Hassan

Sl. NO	USN	Name	signature
25	4JNI6EC007	Anitha K.P.	Anitha K.P.
26	4JNI7EC415	Sevanthi. B.A	Sevanthi
27	4JNI7EC402	Pooja. B	Pooja
28	4JNI6EC038	Kusuma. S.	Kusuma S
29	4JNI6EC046	Meenakshi. N	Meenakshi. N
30	4JNI7EC401	Archana. V	Archana. V

National Education Society(R) Jawaharlal Nehru National College of Engineering, Shimoga

Date:29/3/2019

Internal Quality Assurance Cell(IQAC)

Department of Electronics and Communication Engineering

Institution of Electronics and Telecommunication Engineers, Shivamogga Centre

Industrial Trip to MCF ,Hassan

Dept. of Electronics & Communication Engg. JNNCE SHIVAMOGGA-577 204

SI NO	USN	Name	Signature
1	4JN16EC074	Sampritha.V.Satish	Sampritha
2	4JN16EC108	Usha.HJ	Usha
3	4JN16EC113	Varshitha.C.	Varshitha.C
4	4JN16EC089	Shruthi. G	Shruthi
5	4JN16EC061	Prajwal.R	Prajwal
6	4JN16EC105	Vedavathi.H.A	Veda
07.	4JN16EC109.	V. Shruthi	Shru
8.	4JN16EC104	Tekoor Sapna Ravindrakumar	Ravi
9.	4JN16EC056	Pavithra.D.B	pavithra.D.B
10	4JN16EC069	Rashmi.C.V.	Rashmi.C.V.
11	4JN16EC073	Sahana R	Sahana.R
12.	4JN16EC099	Supriya.G.A	Supriya.G.A
13	4JN16EC078	Sannidhi.M.S	Sannidhi.M.S
14.	4JN16EC100	Sushmitha.S	Sushmitha.S
15.	4JN16EC064	Priyanka.R.J	Priya
16	4JN16EC063	Priyanka.N.	Priyanka.N.
17	4JN16EC066	Rachana S Iyara	Rachana
18		Sangitha.	
19.		Divya.	
20.	4JN16EC116	Vimal.K.M	Vimal
21.	4JN16EC068	Ranjitha.S	Ranj
22.	4JN16EC065	Rachana.B	Rachana.B

National Education Society(R) Jawaharlal Nehru National College of Engineering, Shimoga

Date:29/3/2019

Internal Quality Assurance Cell(IQAC)

Department of Electronics and Communication Engineering

Institution of Electronics and Telecommunication Engineers, Shivamogga Centre

Industrial Trip to MCF ,Hassan

Department of Electronics & Communication Engg. JNNCE SHIVAMOGGA-577 204

Sl No	USN	Name	Signature
1	4JN16EC085	Shreyas.B	Shreyas B
2)	4JN17EC412	Sachin.B	Sachin B
3)	4JN16EC097	Suhas.S	Suhas
4)	4JN16EC106	Tilak Prasad K.M	Tilak
5)	4JN16EC086	Shreyas.J.S.	Shreyas
6)	4JN16EC103	Tejas Kumar.P.N	Tejas
7)	4JN16EC090	Shubhan H.K	
8	4JN16EC077	Sanjay.B.J	Sanjay B J
9	4JN16EC098	Suhas.S.Nair	Suhas
10	4JN16EC110	Vaibhav Jain	Vaibhav Jain

Department of Electronics & Communication Engineering
JNNCE
SHIVAMOGGA-
577 204

Date:30/3/2019

REPORT

The department of Electronics and Communication Engineering of Jawaharlal Nehru National College of Engineering, Shivamogga in association with IETE Shimoga Centre has organized an Industrial trip to Master Control facility, Hassan to 6th semester students of ECE on 29/3/2019. The team lead by Dr.P.Manjunatha ,Professor and Head dept of ECE accompanied by four faculty members Mrs. Ujwala B.S, Mrs.Nalina S.B, Mrs.Shwetha B and Mr. anil Kumar J departed the city at around 7AM on 29/3/2019. Almost 69 students were part of the event.

The team arrived at MCF hassan at 2.00 PM via Belur and Halebidu. Mr.Yesobu Bach ,Sr.Scientist, MCF has delivered an informative lecture on the motive of the Master control facility and also the main theme of the centre.The scientist also explained the details satellites used for different applications and their design aspects. The students got good knowledge about the satellites and the Aerospace Stations. The team left the MCF at 5.30 PM and visited the Pushpagiri on the way and enjoyed the beauty of the place in the evening.

The team returned back safely and reached Shivamogga at 9.30 PM . All students were fascinated and overwhelmed by the visit.

(Dr. P. Manjunatha)
Chairman, IETE Shimoga Centre

office Copy -

NATIONAL EDUCATION SOCIETY (R)

Jawaharlal Nehru National College of Engineering

(Affiliated to Visvesvaraya Technological University & Recognised by AICTE, New Delhi)

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

SHIVAMOGGA - 577 204
KARNATAKA STATE

No. : JNNCE/EE/886/2017-18

Date 27/9/17

To,
The General Manager,
Corporate Communications,
Karnataka Power Corporation Ltd.,
Shakthi Bhavan,
#82, Race course road,
BANGALORE-577435
Ph: 080-22256568,22203709,Fax:22252144

Sir,

Subject: Permission to visit the Vaarahi Power Plant and Mani dam–reg.

With respect to the above subject, about 70 pre-final year B.E. students of our branch, intend to visit the esteemed Vaarahi Power Plant, on 13th Oct'2017, along with the Staff members. This visit will give them a direct practical exposure of a Power plant, which is installed underground. They also intend to visit Mani dam, same day.

Please grant the permission to visit the Power plant and Mani dam.

Thanking You,

Yours faithfully,

Head of the dept.,
E.E.dept., J.N.N.C.E.

Professor and Head
Dept. of Electrcial & Electronics Engg.
Jawaharlal Nehru
National College of Engineering
SHIMOGA-577 204.

Encl: List of visitors.

Contact
Mr. Chandrashekhara S.
98447-62369.

faxed on 27/9/17 @ 1pm and faxed on 27/9/17 @ 4:45 pm

KPCL
ಕರ್ನಾಟಕ ವಿದ್ಯುತ್ ನಿಗಮ ನಿಯಮಿತ
KARNATAKA POWER CORPORATION LTD.
(A premier power generating company of Government of Karnataka)
CIN U85110KA1970SGC001919

ಸಂಖ್ಯೆ:ಎ1 ಎ6 ಎ ಸಿಸಿ:190 /ಬೆಂಗ/2017 ದಿನಾಂಕ: 28-09-2017

ಇವರಿಗೆ:

ಪ್ರಾಂಶುಪಾಲರು.
ಜವಾಹರಲಾಲ್ ನೆಹರು ನ್ಯಾಷನಲ್ ಕಾಲೇಜ್ ಆಫ್ ಇಂಜಿನೀಯರಿಂಗ್.
ಶಿವಮೊಗ್ಗ-577204.
ದೂರವಾಣಿ -08182-276707.

ಮಾನ್ಯರೇ,

ವಿಷಯ: ವಾರಾಹಿ ಯೋಜನಾ ಪ್ರದೇಶವನ್ನು ಸಂದರ್ಶಿಸಲು ಅನುಮತಿ - ಕುರಿತು.

ಉಲ್ಲೇಖ: ನಿಮ್ಮ ಪತ್ರ ಸಂಖ್ಯೆ:JNNCE/EE/886/2017-18 ದಿನಾಂಕ:27-09-2017.

*****

ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು ಸಂದರ್ಶಿಸಲು ತಾವು ಬರೆದುಕೊಂಡ ಉಲ್ಲೇಖ ಪತ್ರದಲ್ಲಿ ತಿಳಿಸಿರುವಂತೆ ಮಾನಿಡ್ಯಾಂ ಪವರ್ ಹೌಸ್/ಮಾಸ್ತಿಕಟ್ಟೆ ಮತ್ತು ವರಾಹಿ ಭೂಗರ್ಭ ಜಲವಿದ್ಯುದಾಗಾರ/ಹೊಸಂಗಡಿ ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು **ದಿನಾಂಕ:13.10.2017**ರಂದು ನಿಮ್ಮ ಸಂಸ್ಥೆಯ ಅಂತಿಮ ವರ್ಷದ ಬಿ.ಇ **66** ವಿದ್ಯಾರ್ಥಿಗಳು ಹಾಗೂ **04** ಉಪನ್ಯಾಸಕರು/ಸಿಬ್ಬಂಧಿ ಸೇರಿ ಒಟ್ಟು **70** ಸದಸ್ಯರಿಗೆ ವೀಕ್ಷಿಸಲು **(afternoon batch)** ಈ ಮೂಲಕ ಅನುಮತಿ ನೀಡಲಾಗಿದೆ.

ಈ ಅನುಮತಿಯು ಕೆಳಗಿನ ನಿಬಂಧನೆಗಳಿಗೆ ಒಳಪಟ್ಟಿರುತ್ತದೆ.

1) ಸಂಸ್ಥೆಯ ಮುಖ್ಯಸ್ಥರಿಂದ ಪಡೆದಿರುವ ಗುರುತಿನ ಚೀಟಿಯನ್ನು (**Identity card**) ಹಾಜರು ಪಡಿಸಲು ಸೂಚಿಸಲಾಗಿದೆ. ಗುರುತಿನ ಚೀಟಿ ಇಲ್ಲದಿದ್ದ ಪಕ್ಷದಲ್ಲಿ ಮುಖ್ಯಸ್ಥರಿಂದ ದೃಢೀಕರಿಸಿರುವ ವಿದ್ಯಾರ್ಥಿಗಳ ಮತ್ತು ಉಪನ್ಯಾಸಕರ ಹೆಸರುಗಳ ಪಟ್ಟಿಯನ್ನು ಕಡ್ಡಾಯವಾಗಿ ಹಾಜರು ಪಡಿಸಲು ಸೂಚಿಸಲಾಗಿದೆ.

2) ಪಟ್ಟಿಯಲ್ಲಿರುವವರನ್ನು ಭಾರತೀಯ ಪೌರರೆಂದು ಧೃಢೀಕರಿಸಬೇಕು. ಇಲ್ಲದ ಪಕ್ಷದಲ್ಲಿ ಅನುಮತಿಯನ್ನು ನಿರಾಕರಿಸಲಾಗುವುದು. ವಿದೇಶಿಯರಿಗೆ ಯೋಜನಾ ಪ್ರದೇಶಗಳಿಗೆ ಅನುಮತಿ ನೀಡಲಾಗುವುದಿಲ್ಲ.

3) ವಿಡಿಯೋ/ಮೊಬೈಲ್/ಕ್ಯಾಮರಗಳನ್ನು ಯೋಜನಾಪ್ರದೇಶದ ಒಳಗೆ ತೆಗೆದುಕೊಂಡು ಹೋಗುವುದನ್ನು ಹಾಗೂ ಛಾಯಾಚಿತ್ರಗಳನ್ನು, ಸೆಲ್ಫಿ ತೆಗೆಯುವುದನ್ನು ನಿಷೇಧಿಸಲಾಗಿದೆ.

4) ವಿದ್ಯಾರ್ಥಿಗಳು **16**ವರ್ಷ ಮೇಲ್ಪಟ್ಟವರಾಗಿದ್ದು ಸಂಸ್ಥೆ/ಕಾಲೇಜು ಮುಖ್ಯಸ್ಥರುಗಳು ಕಡ್ಡಾಯವಾಗಿ ತಂಡದೊಂದಿಗೆ ಇರಬೇಕು. ವಿದ್ಯಾರ್ಥಿಗಳ ರಕ್ಷಣೆಯ ಜವಾಬ್ದಾರಿ ಸಂಸ್ಥೆ/ಕಾಲೇಜಿನ ಮುಖ್ಯಸ್ಥರುಗಳಿಗೆ ಸೇರಿರುತ್ತದೆ.

5) ಯೋಜನಾ ಪ್ರದೇಶದಲ್ಲಿ ಆಹಾರ ಸ್ವೀಕರಿಸುವುದು, ಮನೋರಂಜನೆ ಮತ್ತು ಖಾಸಗಿ ವಾಹನಗಳಿಗೆ ಅವಕಾಶವಿರುವುದಿಲ್ಲ.

6) ಯೋಜನಾ ಪ್ರದೇಶದಲ್ಲಿ ನಿಗಮದ ಯಾವುದೇ ಆಸ್ತಿ-ಪಾಸ್ತಿಗೆ ಹಾನಿ ಉಂಟುಮಾಡುವಂತಿಲ್ಲ. ಯಾವುದೇ ಅಹಿತಕರ ಘಟನೆಗಳು ಸಂಭವಿಸಿದಲ್ಲಿ ಸಂಸ್ಥೆಯ/ಕಾಲೇಜಿನ ಮುಖ್ಯಸ್ಥರು ಸಂಪೂರ್ಣ ಜವಾಬ್ದಾರರಾಗಿರುತ್ತಾರೆ. ನಿಗಮ ಯಾವುದೇ ರೀತಿಯಲ್ಲಿ ಜವಾಬ್ದಾರಿಯನ್ನು ಹೊಂದಿರುವುದಿಲ್ಲ.

ತಾವುಗಳು ಯೋಜನಾ ಪ್ರದೇಶಗಳನ್ನು ಪ್ರವೇಶಿಸಿದ ನಂತರ ಭೇಟಿಯ ವ್ಯವಸ್ಥೆಗಾಗಿ ಕಾರ್ಯನಿರ್ವಾಪಕ ಇಂಜಿನೀಯರ್ (ಸಿವಿಲ್) ವಾರಾಹಿ ಯೋಜನಾ ಪ್ರದೇಶಕರು (ಹೈಡಲ್) ವರಾಹಿ, ಹೊಸಂಗಡಿ, ಉಡುಪಿ ಜಿಲ್ಲೆ ದೂರವಾಣಿ ಸಂಖ್ಯೆ: 08259-288242 ಇವರನ್ನು ಸಂಪರ್ಕಿಸುವುದು.

ತಮ್ಮ ವಿಶ್ವಾಸಿ,

ವಂದನೆಗಳೊಂದಿಗೆ,

ಕರ್ನಾಟಕ ವಿದ್ಯುತ್ ನಿಗಮ ನಿಯಮಿತದ ಪರವಾಗಿ,

ಉಪ ಪ್ರಧಾನ ಪ್ರಬಂಧಕರು (ಕಾರ್ಪೊರೇಟ್ ಕಮ್ಯುನಿಕೇಷನ್ಸ್)

ಬಿ.ವಿ. ನಾಯಕ್
ಉಪ ಪ್ರಧಾನ ಪ್ರಬಂಧಕರು
(ಸಾಂಸ್ಥಿಕ ಸಂವಹನ)
#82, 'ಶಕ್ತಿ ಭವನ' ರೇಸ್ ಕೋರ್ಸ್ ರಸ್ತೆ,
ಬೆಂಗಳೂರು - 560 001

'ಶಕ್ತಿ ಭವನ', ನಂ. 82, ರೇಸ್ ಕೋರ್ಸ್ ರಸ್ತೆ, ಬೆಂಗಳೂರು-560 001. ದೂರವಾಣಿ : 080-2225 6568 ಫ್ಯಾಕ್ಸ್ : 080-2225 2144
'Shakthi Bhavan', # 82, Race Course Road, Bangalore-560 001. Tel. : 080-2225 6568 Fax : 080-2225 2144
E-mail : kpclcccmpa@karnatakapower.com Website : www.karnatakapower.com

List of the Students and Staff members visiting VAARAHI POWER HOUSE and MANI DAM

Date: 27-09-2017

5th EE Students list:

Sl.No	Name of the Student	USN
1	Pooja B	4JN13EE030
2	Dashami T	4JN14EE014
3	Mohammed Farooq H S	4JN14EE023
4	*Afreen Taj K H	4JN15EE001*
5	Anitha K S	4JN15EE002
6	Ankitha R	4JN15EE003
7	*Architha S	4JN15EE005*
8	Ashwin S	4JN15EE006
9	Bhoomika S Gudigar	4JN15EE008
10	*Chaitra G B	4JN15EE009*
11	*Deekshitha T K	4JN15EE011*
12	Divya Laxman Harmalkar	4JN15EE012
13	Divyajyothi M	4JN15EE013
14	Dixith B	4JN15EE014
15	G B Shashikumar	4JN15EE015
16	Ganeshprasad M R	4JN15EE016
17	Gayitri N	4JN15EE017
18	*Harshith C	4JN15EE018*
19	*Hemashree E	4JN15EE019*
20	Kavya N	4JN15EE021
21	Likitha A	4JN15EE022
22	Madhukar K E	4JN15EE023
23	Manoranjan R	4JN15EE024
24	Megha C R	4JN15EE025
25	Megha H R	4JN15EE027
26	Nireeksha H N	4JN15EE028
27	Patsy Smitha Lobo	4JN15EE030
28	Priya S M	4JN15EE032
29	Rachana S V	4JN15EE035
30	Rakesh Kumar R	4JN15EE036
31	Ranjitha G	4JN15EE037
32	Rukshana M S	4JN15EE038
33	Samreen Banu (##)	4JN15EE040
34	Sharathkumar Goudar	4JN15EE041
35	Shreedhar Rao N R	4JN15EE043
36	Siddharthini H M	4JN15EE044
37	Sumanth N	4JN15EE045
38	*Sunitha C	4JN15EE046*

27/9/17

Professor and Head
Dept. of Electrcial & Electronics Engg.
Jawaharlal Nehru
National College of Engineering
SHIMOGA-577 204.

Page 2e (1) & (2)

27/9/17

39	Suprith M	4JN15EE048
40	Supriya S	4JN15EE049
41	Sushmam D	4JN15EE050
42	Syed Ebadur Rahman	4JN15EE051
43	*Syed Imran	4JN15EE052*
44	Vidya H	4JN15EE053
45	Vinayaka B S	4JN15EE055
46	*Wasim Akram	4JN15EE056*
47	Yashas B U	4JN15EE057
48	Zakeeya	4JN15EE058
49	Abhishek M	4JN16EE400
50	Ajjaiah G	4JN16EE401
51	Charan Singh	4JN16EE402
52	Girish Shet	4JN16EE403
53	Guruprasad K O	4JN16EE404
54	Karthik V	4JN16EE405
55	Kushal B	4JN16EE406
56	Md. Zakeerulla T Z	4JN16EE407
57	Pradeep K H	4JN16EE408
58	Rakshitha K	4JN16EE409
59	Roopa chavan	4JN16EE410
60	Samarth M S	4JN16EE411
61	Seema N	4JN16EE412
62	Sindhushree S	4JN16EE413
63	Suneeta Maharudrappa B	4JN16EE414
64	Sushmitha C M	4JN16EE415
65	Swaroop S V	4JN16EE416
66	Yashaswini V	4JN16EE417

List of the Staff members:

1	Mr.Chandrashekhara. S	**Phone: 9844762369**
2	Mr.N.G.Ajjanna	**9686799389.**
3	Ms. N.P.Suneetha	
4	Mr.Vidyashankar. M	

27/3/17

Professor and Head
Dept. of Electrcial & Electronics Engg.
Jawaharlal Nehru
College of Engineering

National Education Society ®
JAWAHARLAL NEHRU NATIONAL COLLEGE OF ENGINEERING, SHIVAMOGGA
Department of Information Science & Engineering

Report on Industrial visit 2018-19

An industrial visit was scheduled for the students of 6th semester, information science and engineering on 04/05/2019 to "DXC Technology" IT SEZ Nidige, Machenahallli, Shimoga to enhance the student's knowledge on advanced IT technology. 72 students visited the industry.

Students became more aware of industry practices and regulations during this industry visit. A session on diversified technologies like Java, Android, Python and Cloud Computing was given by Rashmi Suryanarayana, the technical head from DXC Technology. They motivated the students to select their domain, area of interest and also guided the students to select the areas like web development, mobile application development, software testing and its importance in the current software market. She gave a brief introduction of DXC Technology to the students.

The session was concluded with Question-Answer session. After technical talk students interacted with technical head on current demanding technologies, market scenarios. Students were taken on rounds to various departments in industry and briefed on working of various departments in DXC technology. They cleared all the doubt and myths which was in students mind about the technologies and IT sector. All students were satisfied after the session. An overwhelming response was given by the students after this industry visit. The faculty who accomponied expressed thanks to the technical head and all the team members of DXC Technology,who spent their valuable time with students.

Mr. Chethan G S

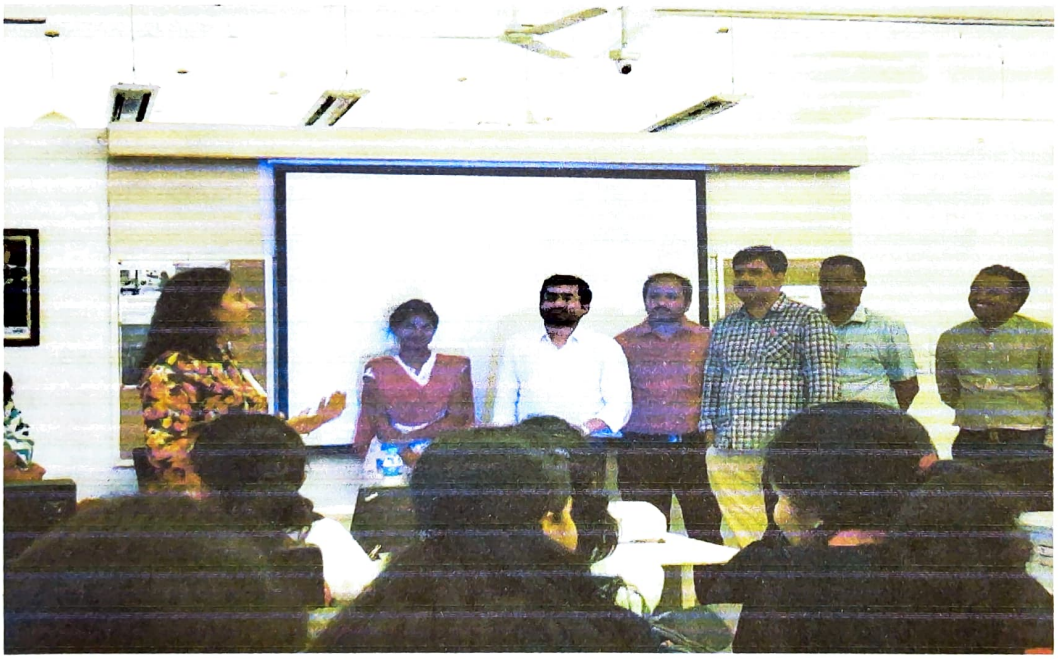
Assistant Professor

Dept.of IS&E.

Professor and Head
Dept. of Information Science & Engg
J.N.N.College of Engineering
SHIMOGA - 577 204

National Education Society ©
JAWAHARLAL NEHRU NATIONAL COLLEGE OF ENGINEERING, SHIVAMOGGA
Department of Information Science & Engineering

Interaction with Students and Faculties



National Education Society ®
JAWAHARLAL NEHRU NATIONAL COLLEGE OF ENGINEERING, SHIVAMOGGA
Department of Information Science & Engineering

Session on diversified technologies

National Education Society ®
JAWAHARLAL NEHRU NATIONAL COLLEGE OF ENGINEERING, SHIVAMOGGA
Department of Information Science & Engineering

Group photo @ DXC Technology